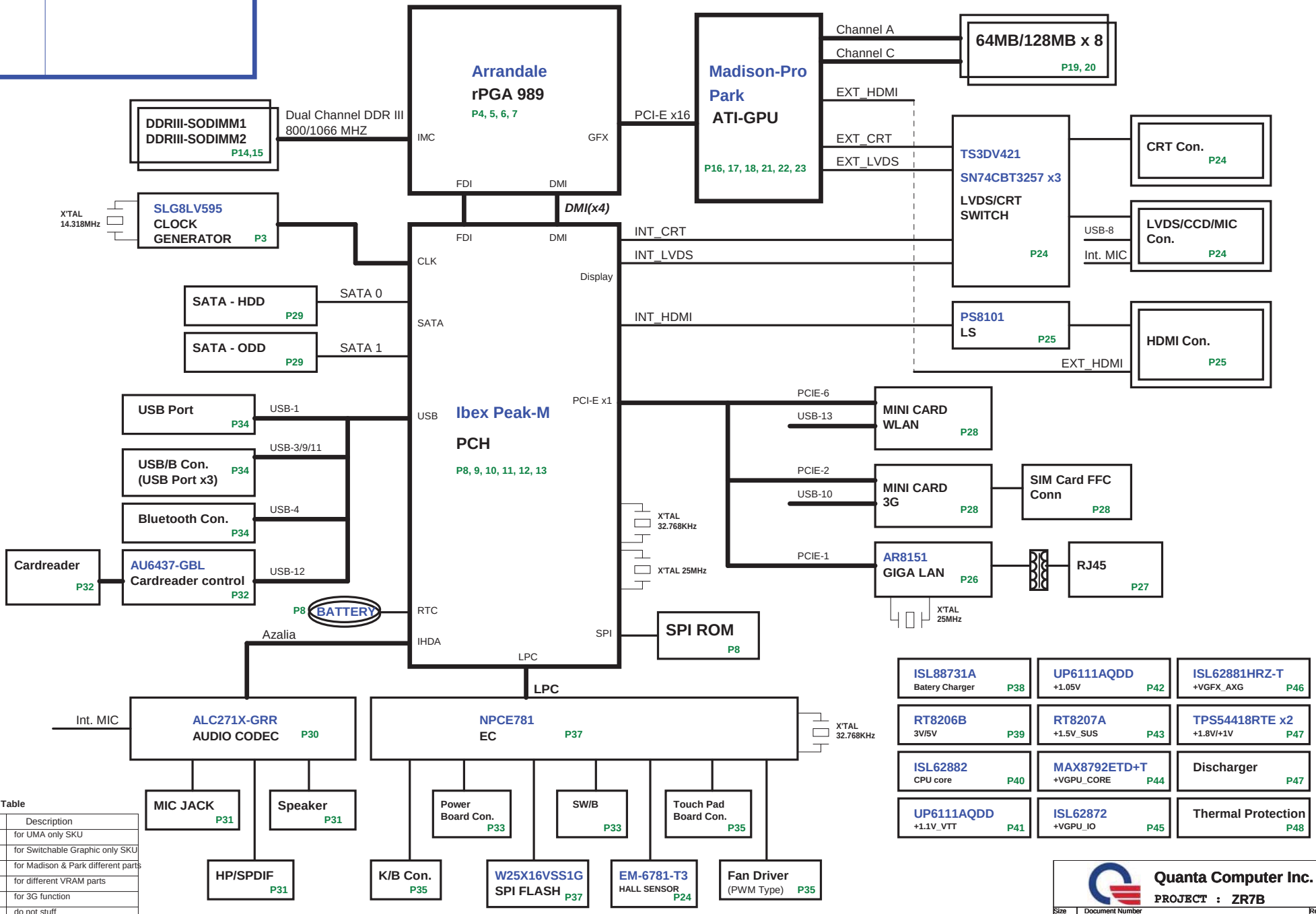
VER : 1A

BOM P/N	Description
31ZR7MB0000	ZR7B MB(UMA,BT)W/O CPU
31ZR7MB0010	ZR7B MB(SG,MADS,SAM,BT,3G)W/O CPU

ZR7B SYSTEM BLOCK DIAGRAM



BOM Option Table

Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU
MP@	for Madison & Park different parts
VRAM@	for different VRAM parts
3G@	for 3G function
*	do not stuff

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Size	Document Number	Rev
	Block Diagram	1A

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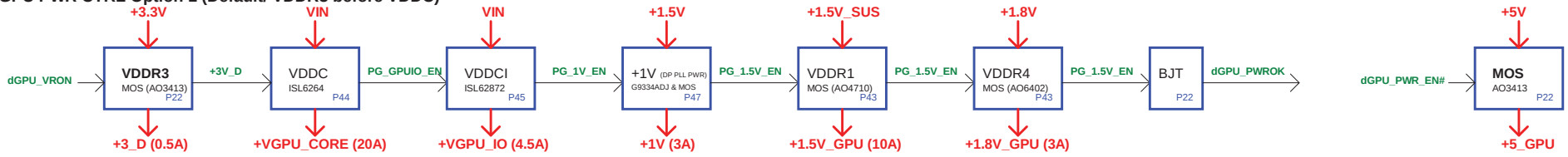
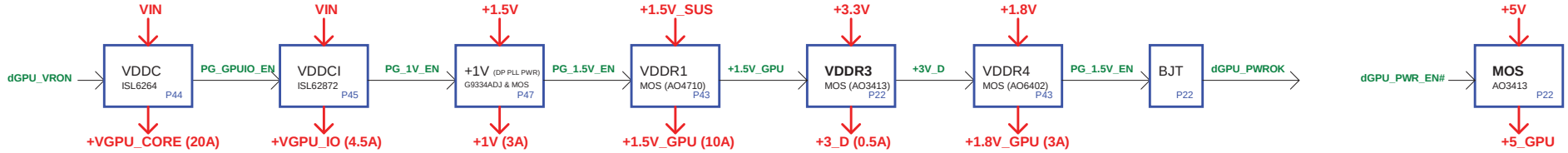
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



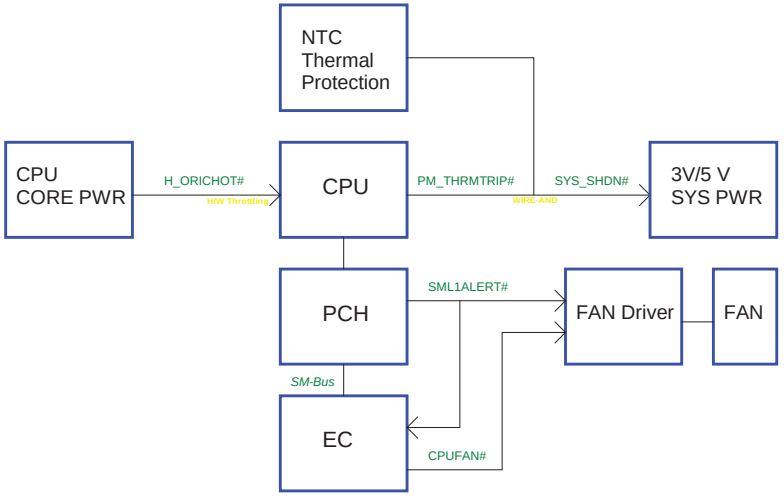
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

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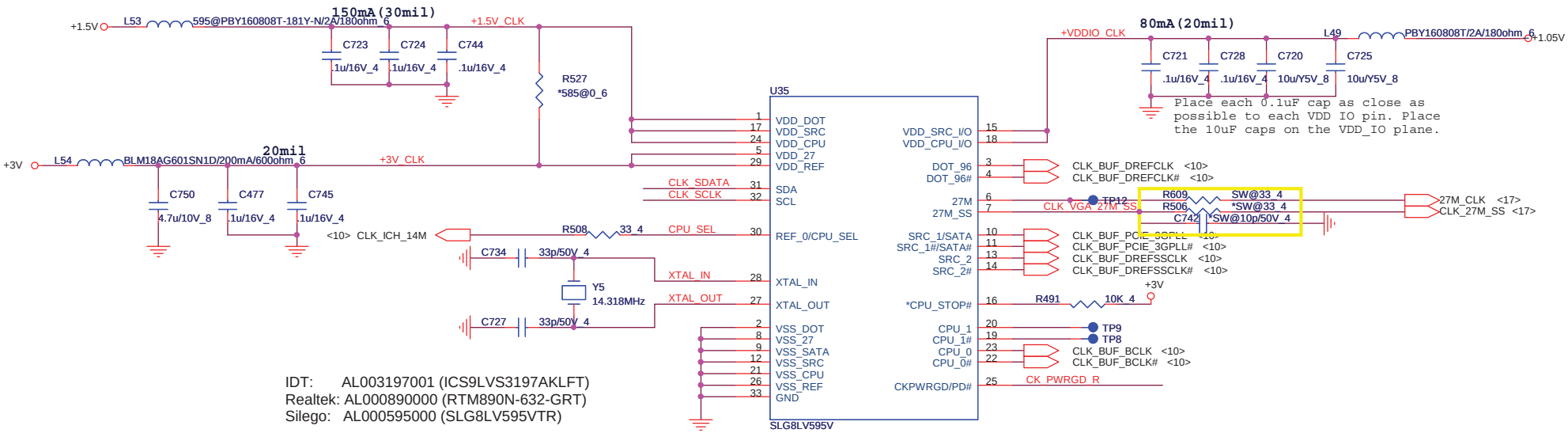
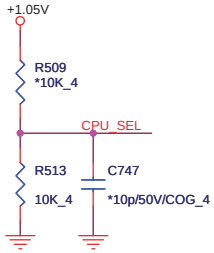


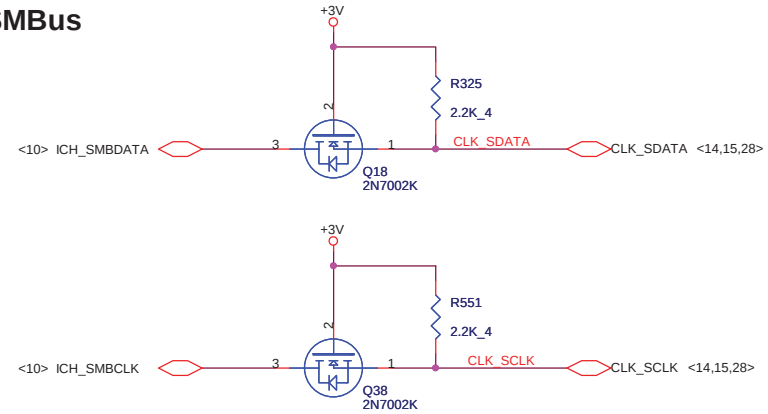
IDT: AL003197001 (ICS9LVS3197AKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select

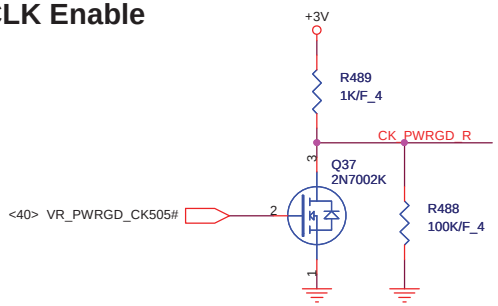


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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	Clock Generator	1A

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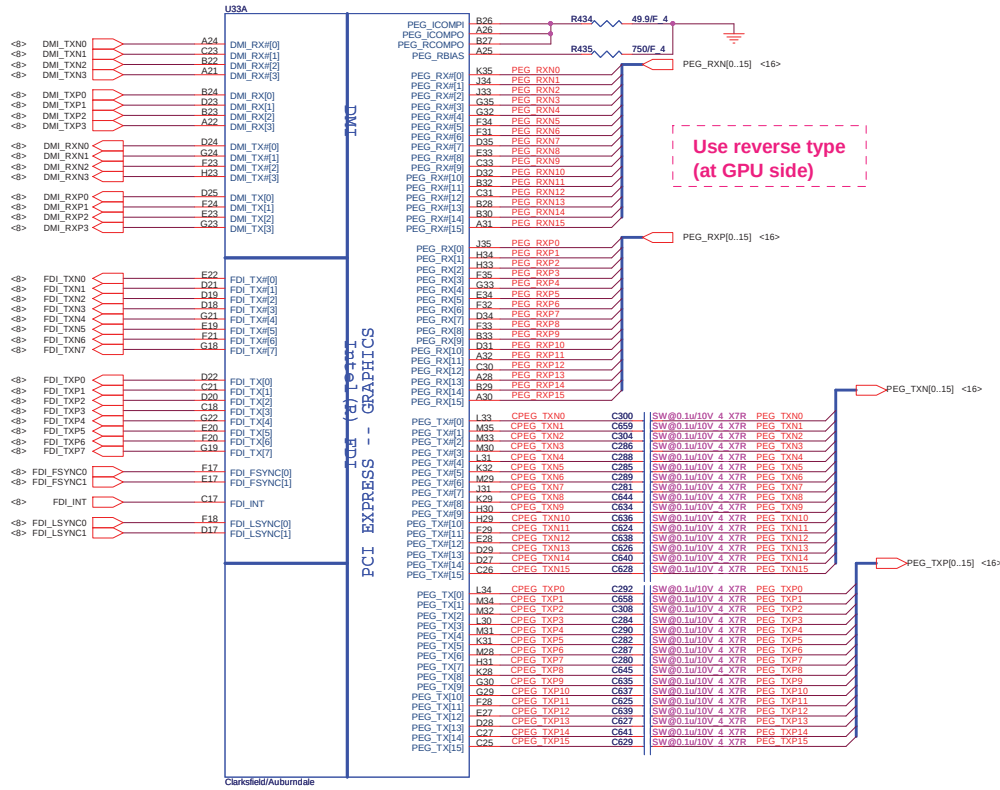
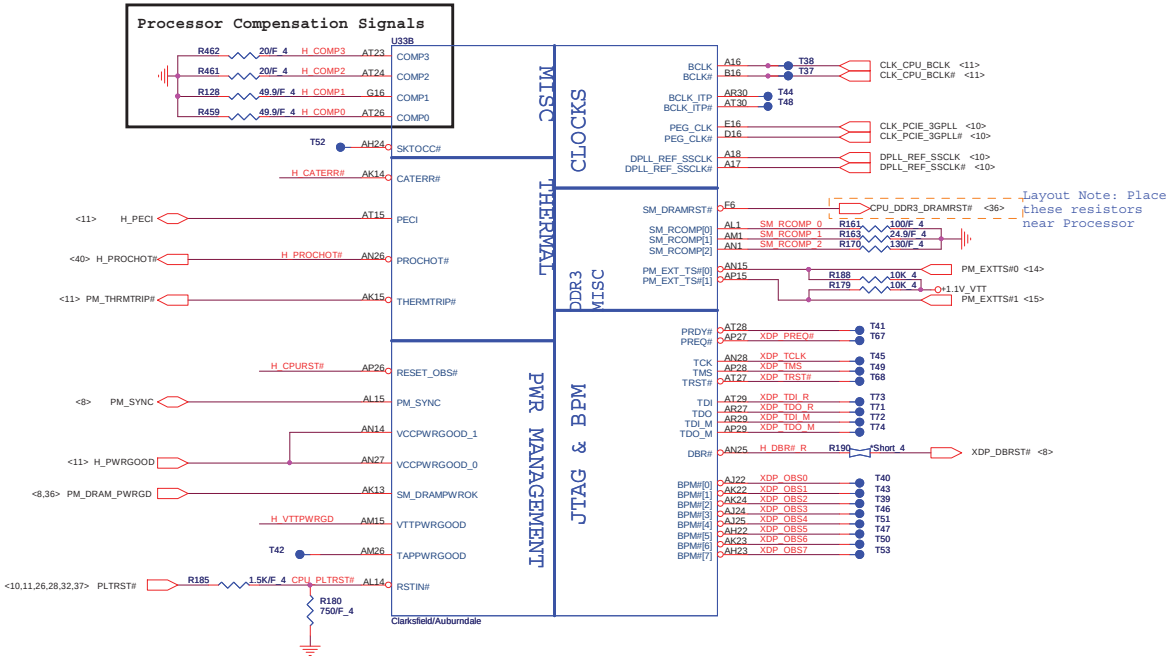
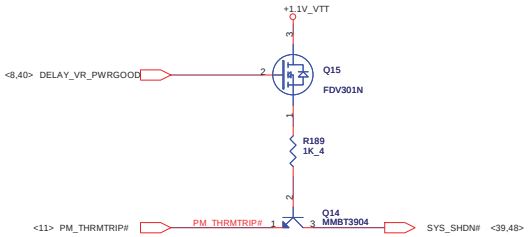
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



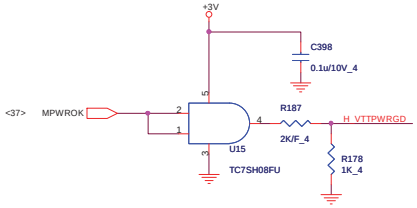
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



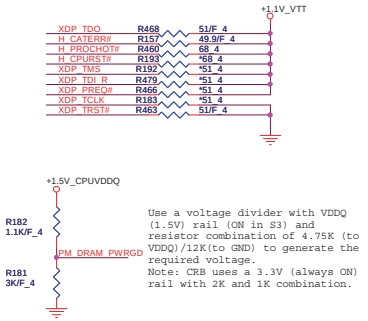
Thermaltrip protect



VTT PWR_Good

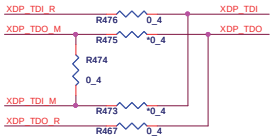


Processor pull-up



Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R497 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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	AUBURNDA 1/4	1A

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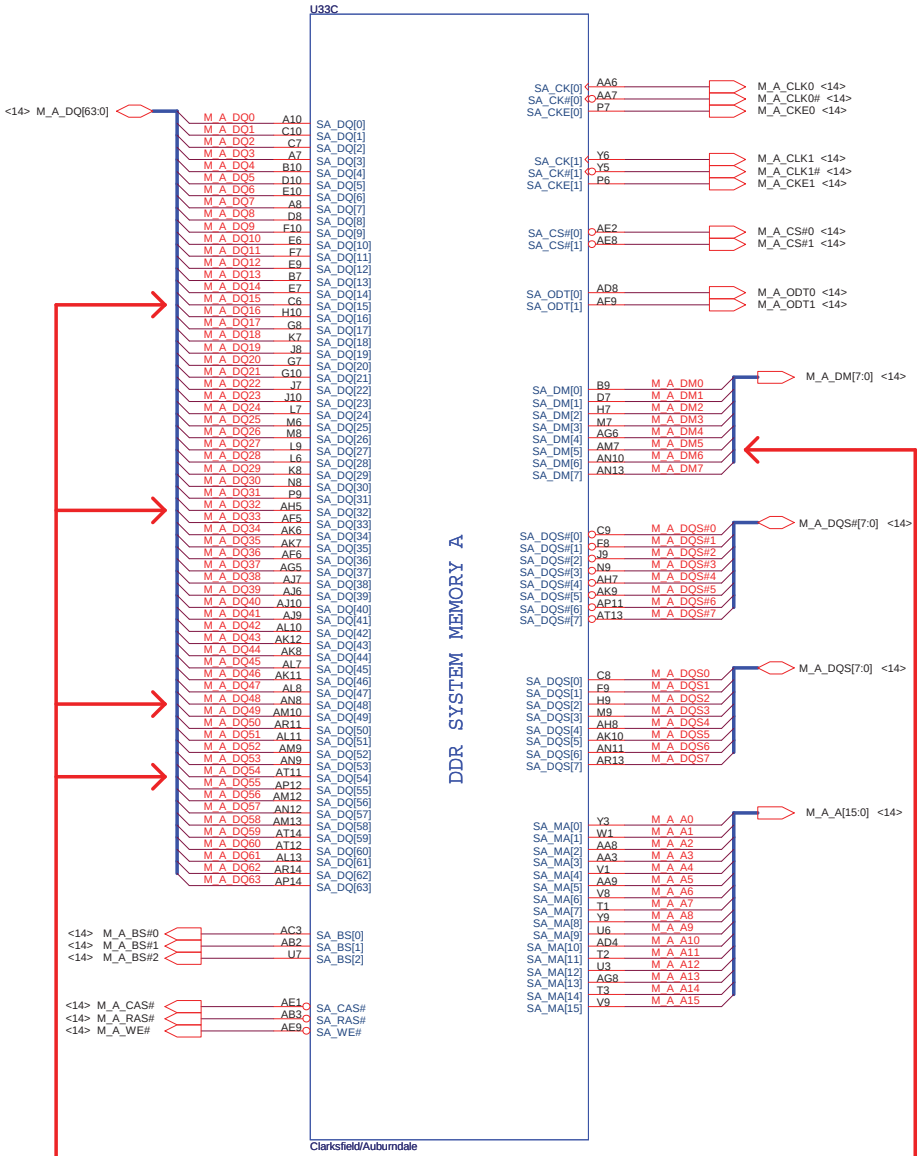
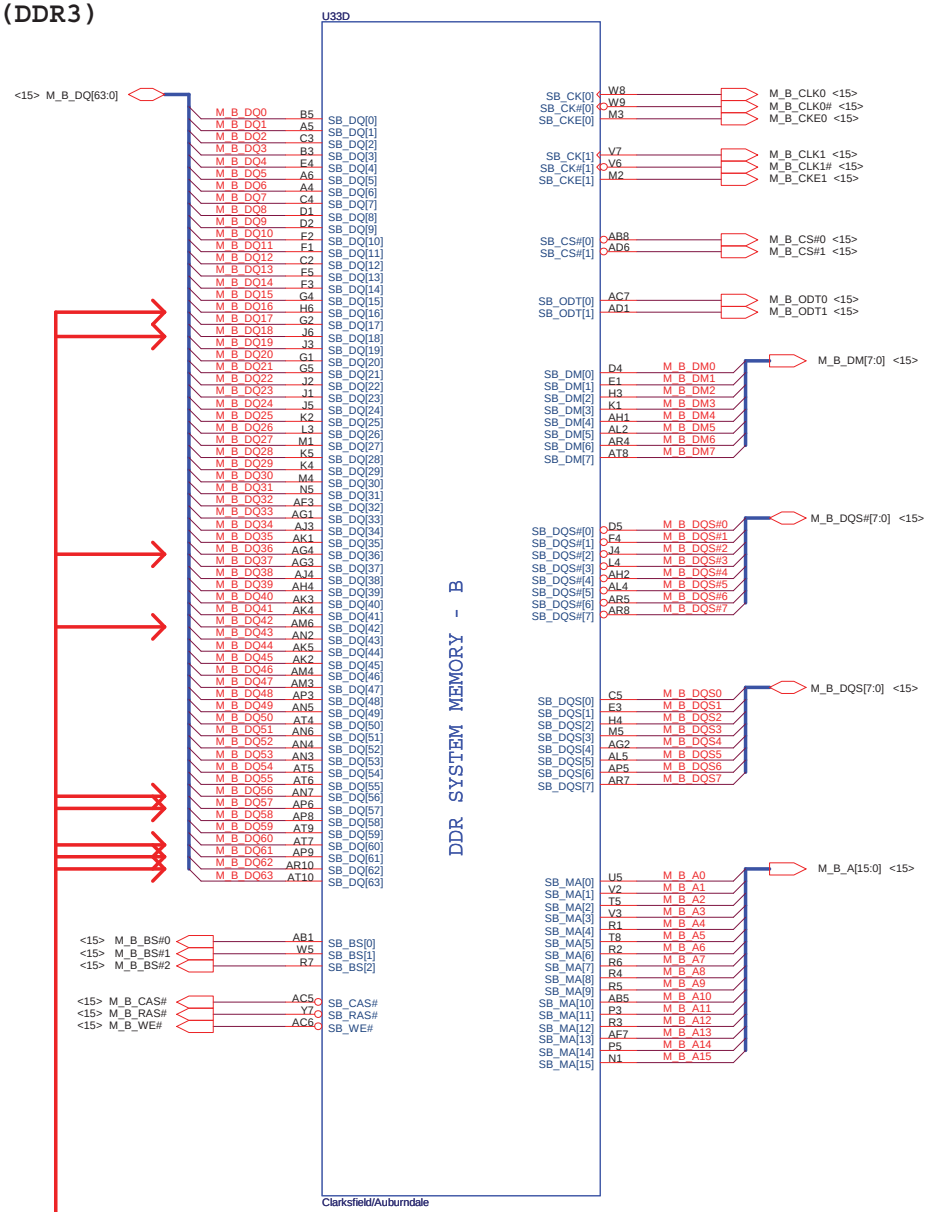
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





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	AUBURNDA 2/4	1A

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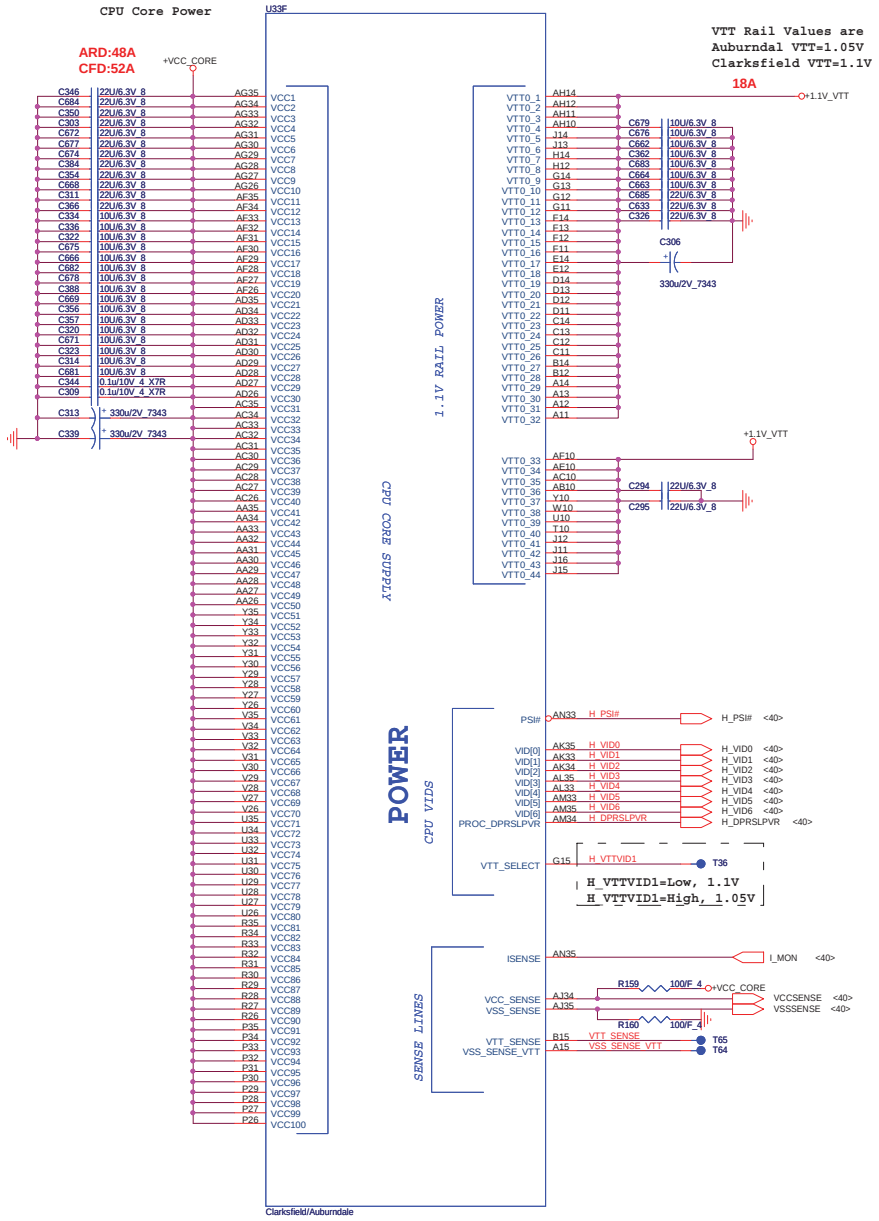
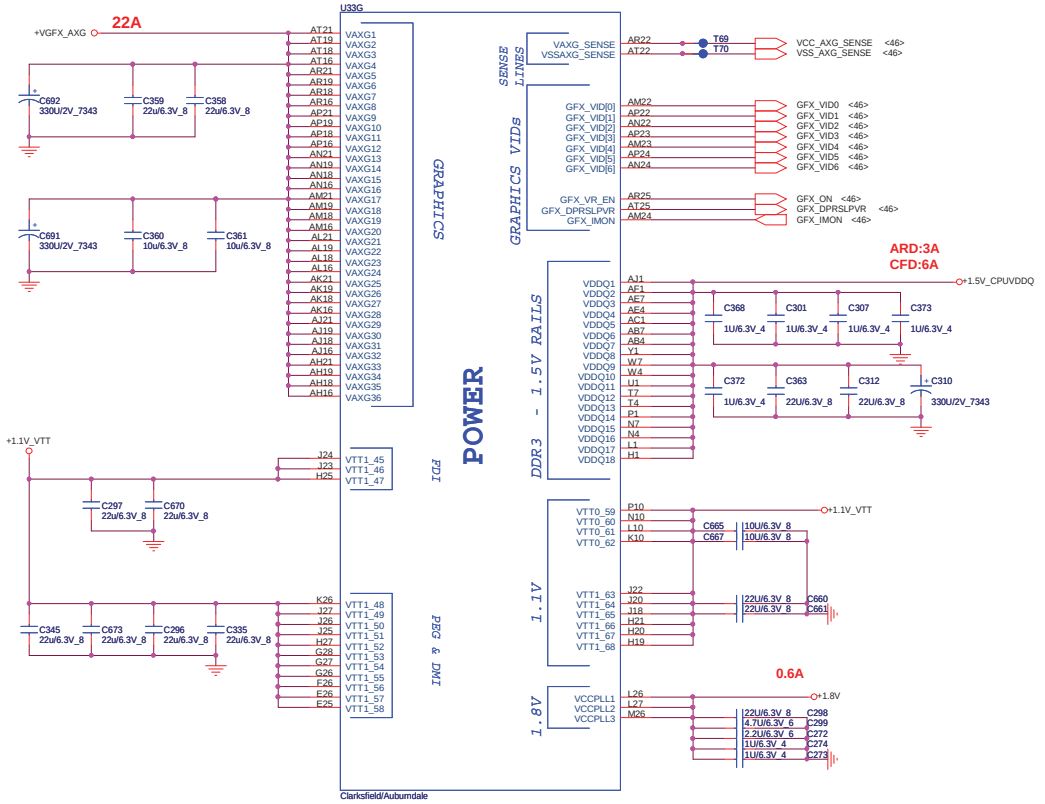
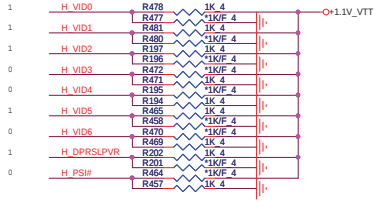


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)





Note:
For Validating IMVP VR R6451 should be STUFF and R2N1 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

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	AUBURNDA 3/4 (PWR)	1A

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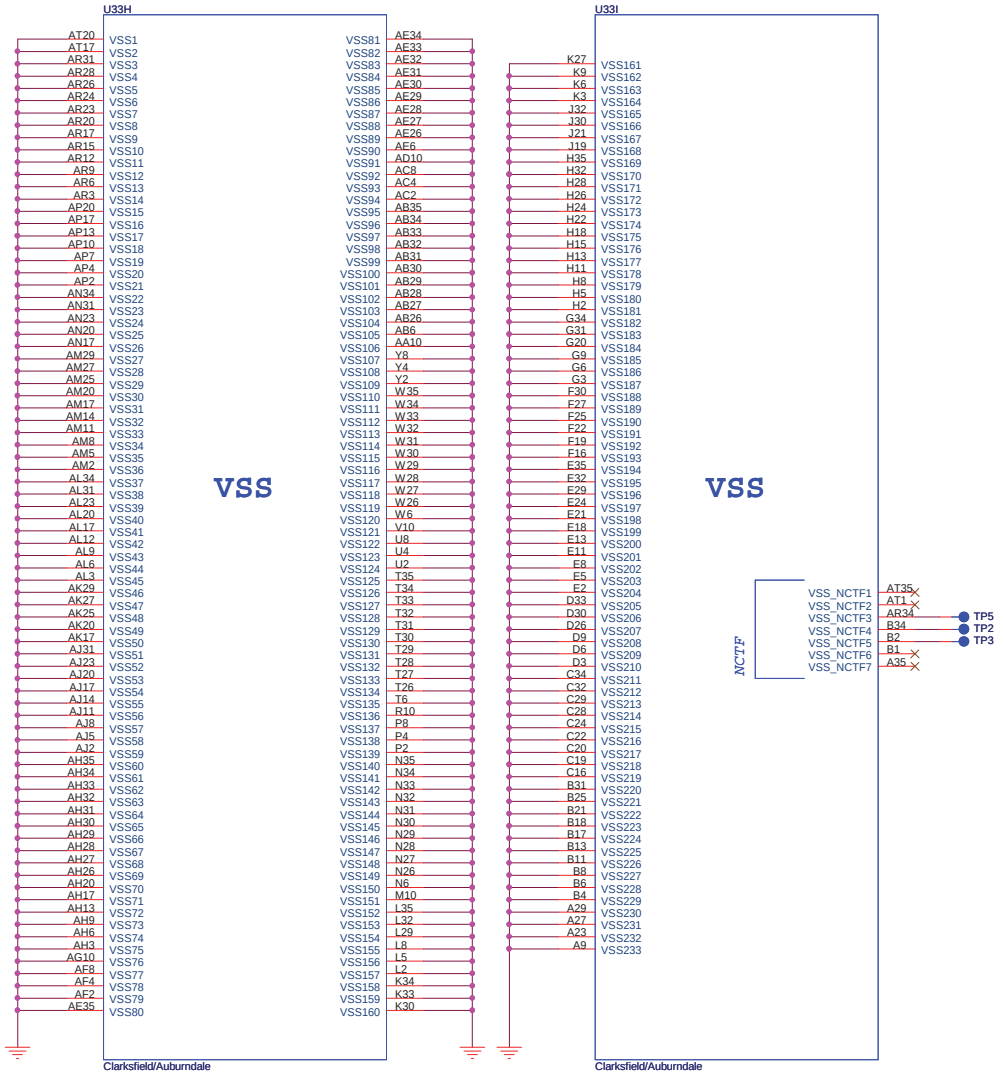
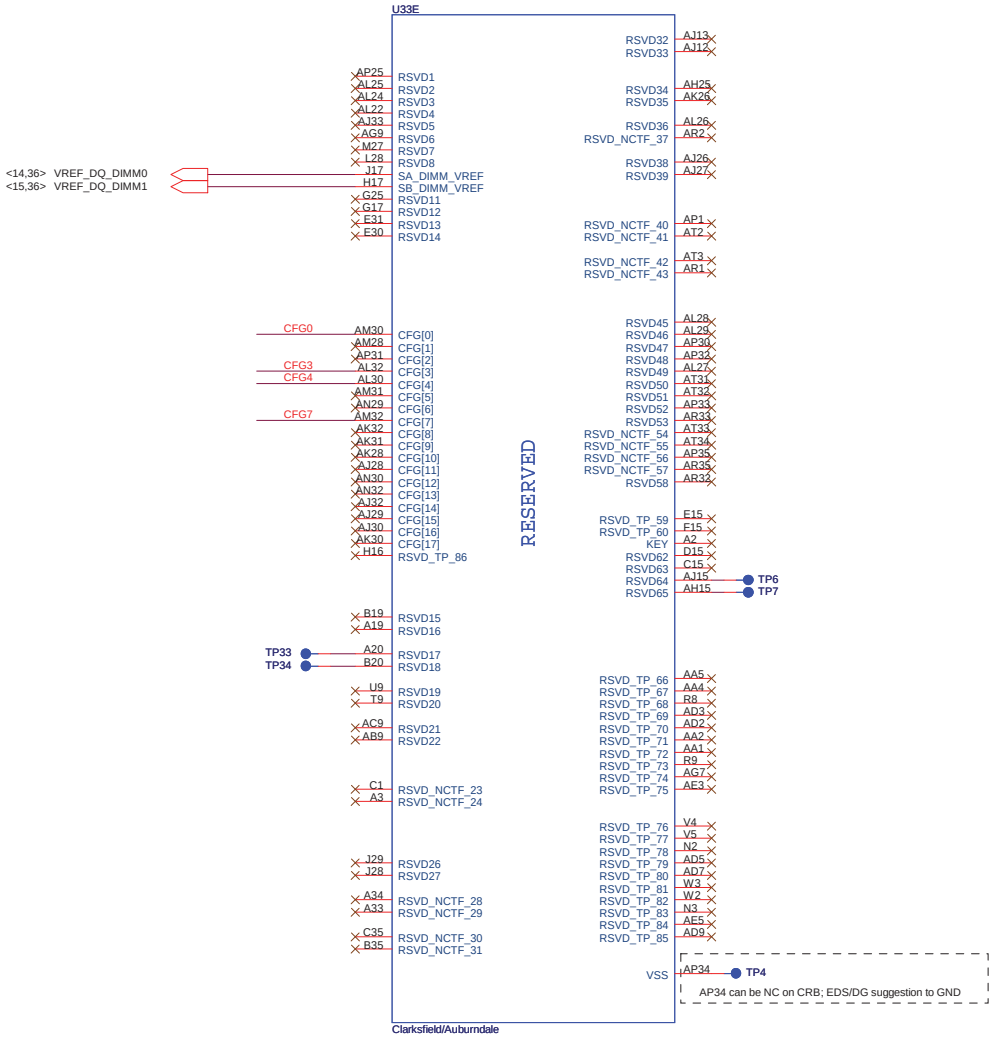
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R186 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R169 3.01K/F_4
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R162 *3.01K
T h e e c d B1 B P R				CFG7 R172 *3.01K/F_4

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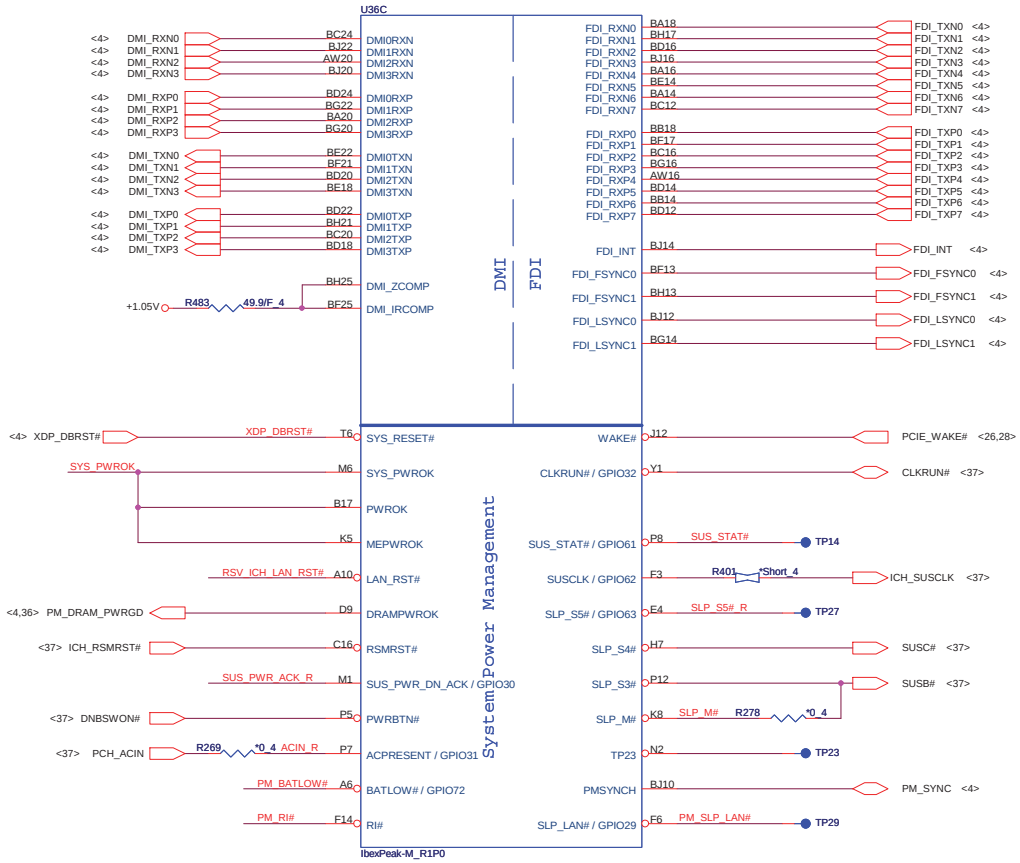
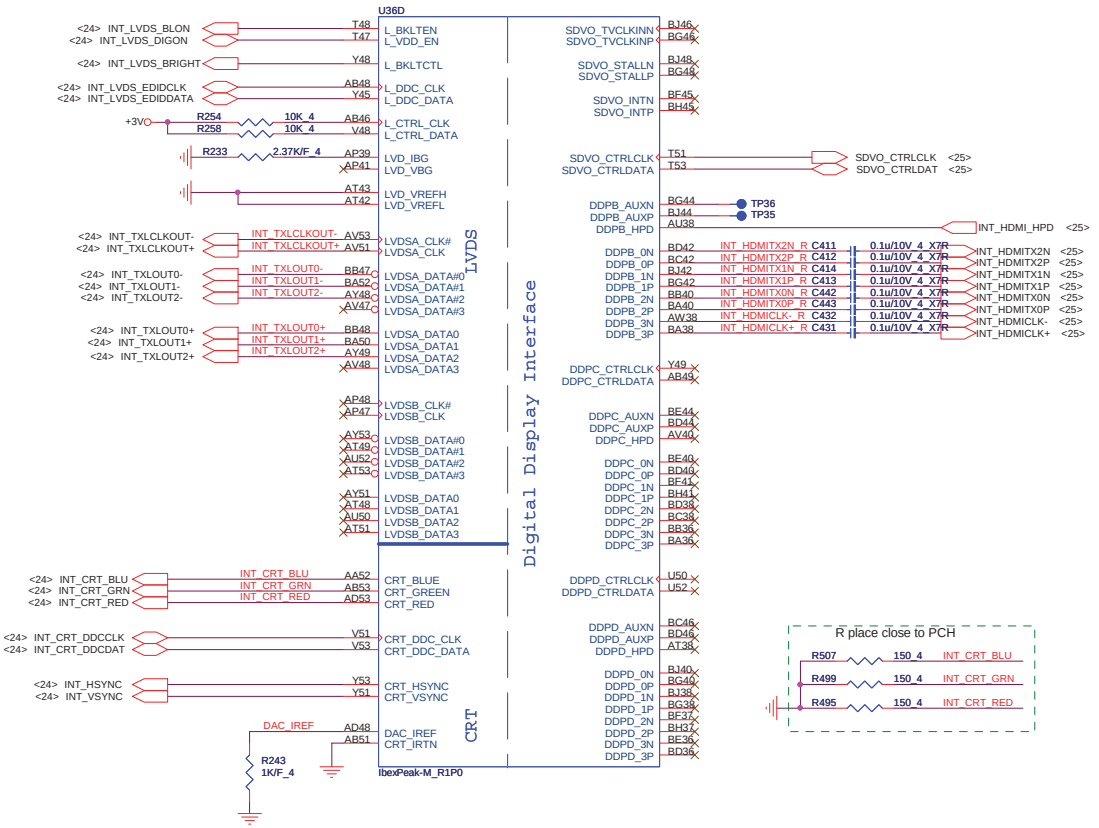
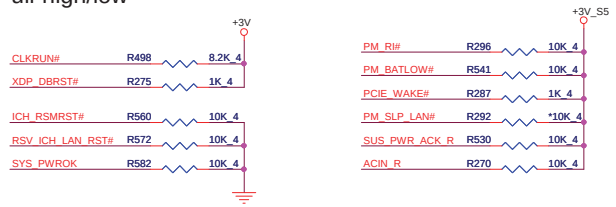
IBEX PEAK-M (DMI,FDI,GPIO)



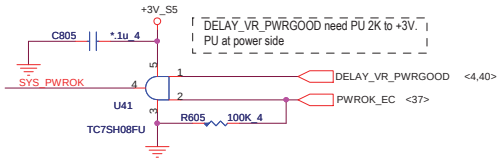
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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	IBEX PEAK-M 1/6	1A

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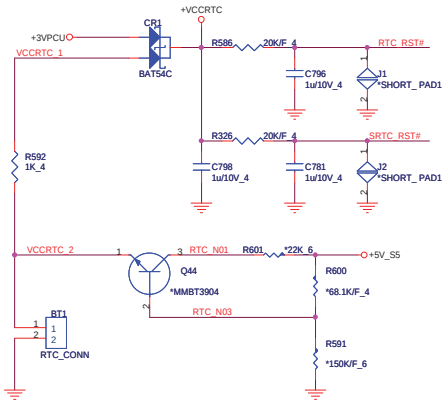
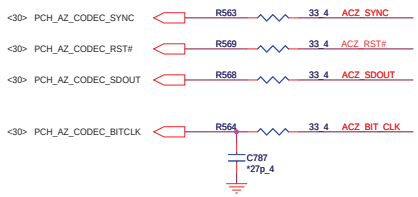
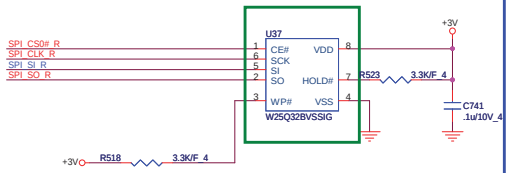
RTC Circuitry

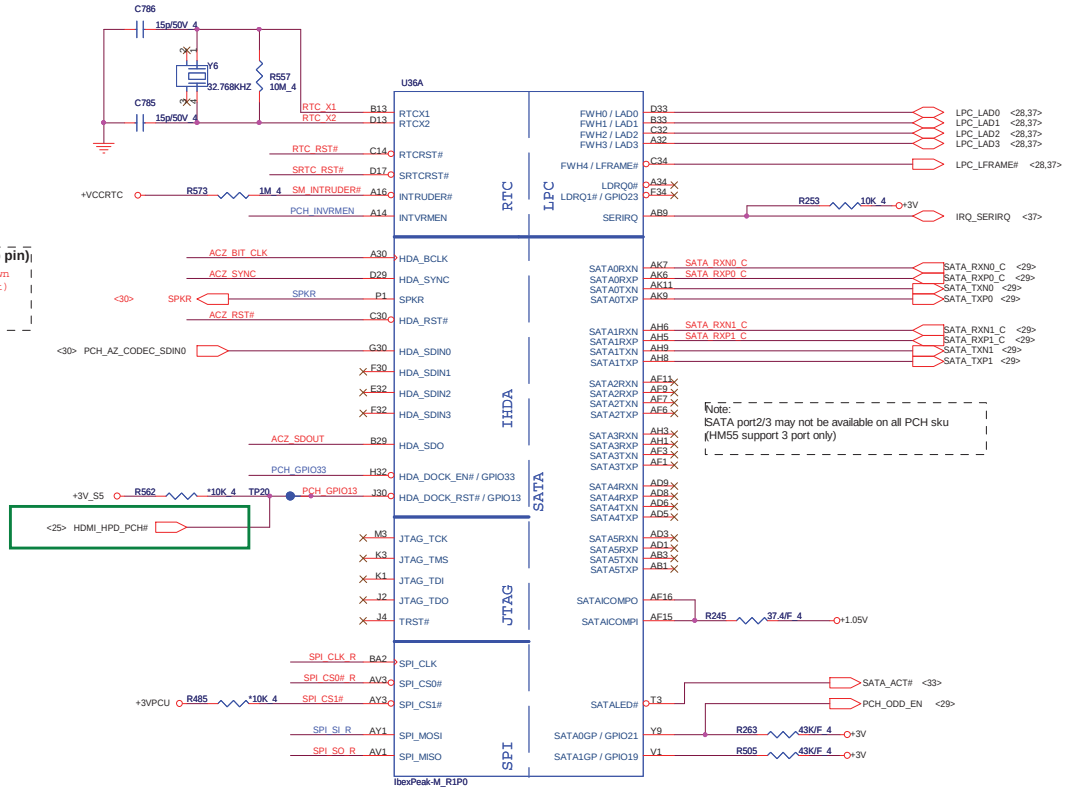


HDA Bus



PCH SPI





PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R593 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R529 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R522 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R286 *1K/F_4 R293 *10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R455 1K_4 R612 1K_4 +3V <10> PCI_GNT0# R282 *1K_4 <10> PCI_GNT1# R285 *1K_4
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10,24> PWM_SELECT# R289 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<30> PCI_GNT3# R528 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	<10> NV_ALE R225 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> NV_CLE R224 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	<11> RSV_GPIO8 R302 10K_4 +3V_S5 R295 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	<11> CR_WAKE# R266 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<11> PCH_GPIO27 R247 *10K_4

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	IBEX PEAK-M 2/6	1A

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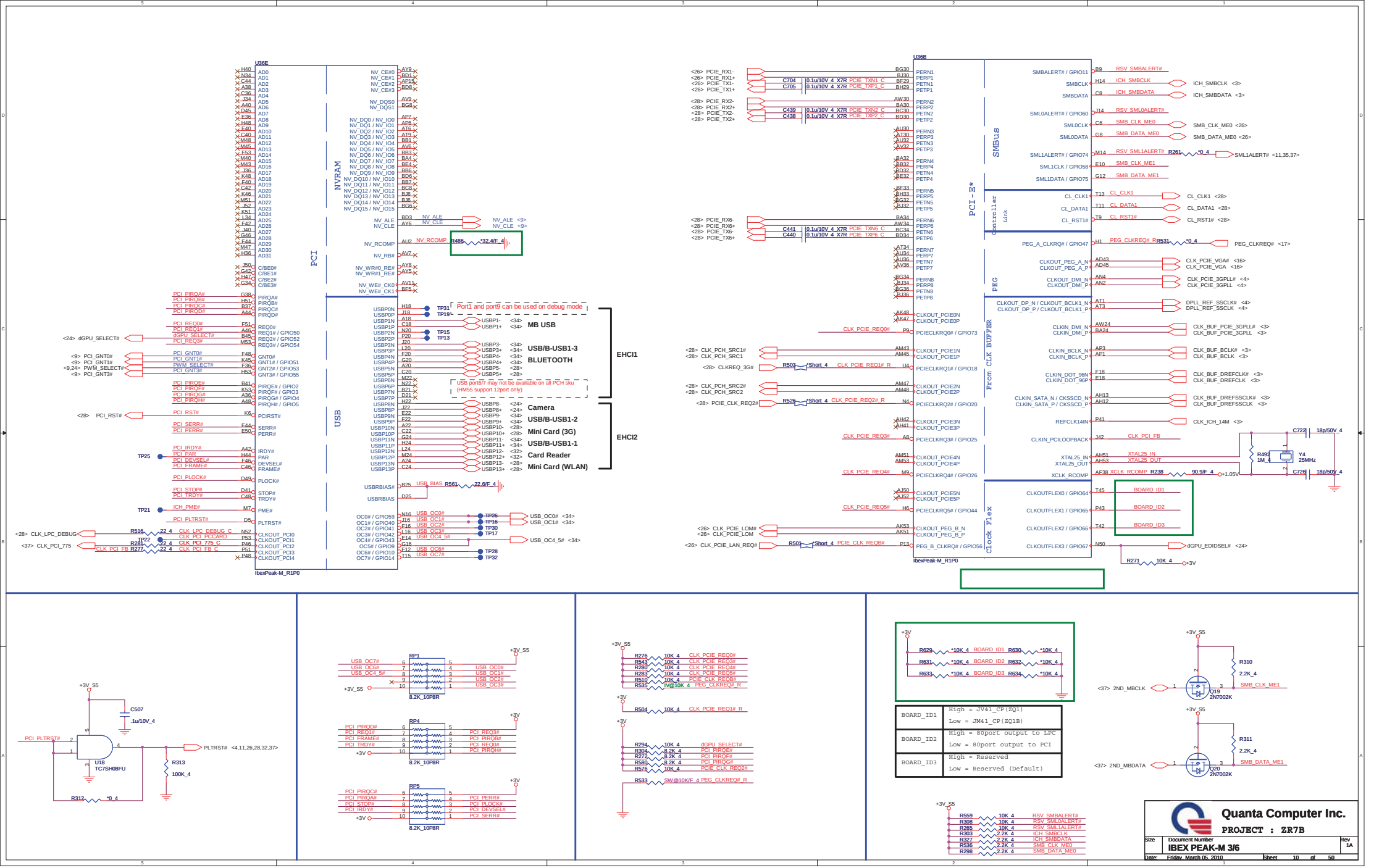
U36E
PCI
NVRAM
USB
IbexPeak-M_R1P0
U36B
PCI-E*
SMBus
Controller Link
PEG
Prom CLK BUFFER
Clock Flex
Port1 and port9 can be used on debug mode
USB port67 may not be available on all PCH sku (HM55 support 12port only)
MB USB
USB/B-USB1-3
BLUETOOTH
EHCI1
Camera
USB/B-USB1-2
Mini Card (3G)
USB/B-USB1-1
Card Reader
Mini Card (WLAN)
EHCI2
Y4 25MHz
BOARD_ID1
BOARD_ID2
BOARD_ID3
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Document Number
IBEX PEAK-M 3/6
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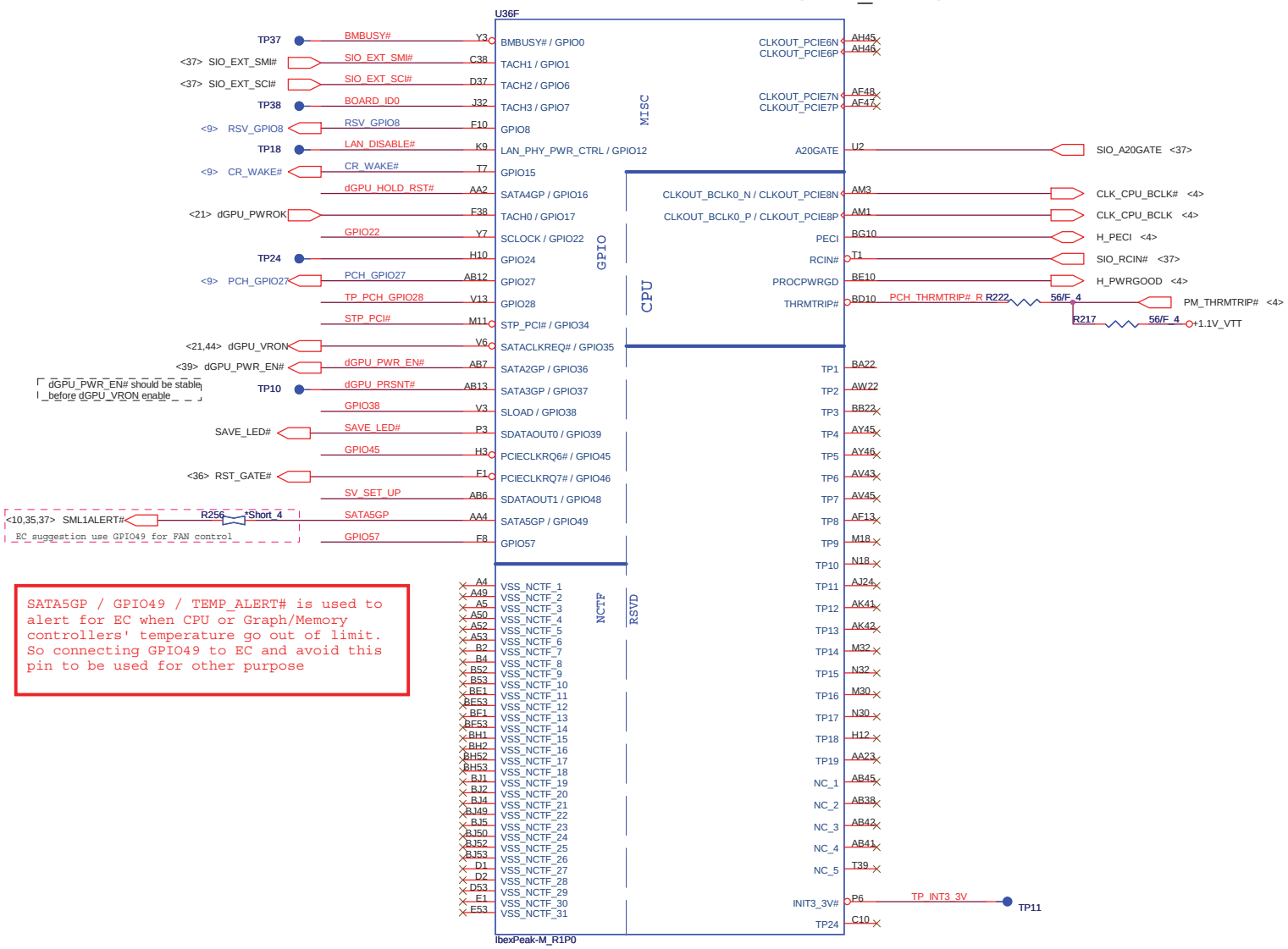
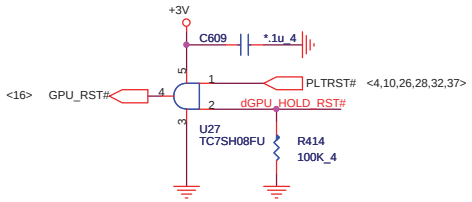
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

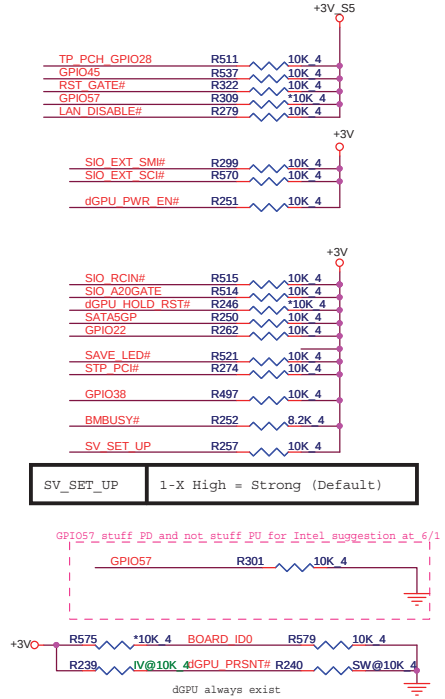


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

BOARD_ID0	High = JV41/JM41 Low = JM51
RSV_GPIO8	High = Disable Low = Enable

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	IBEX PEAK-M 4/6	1A

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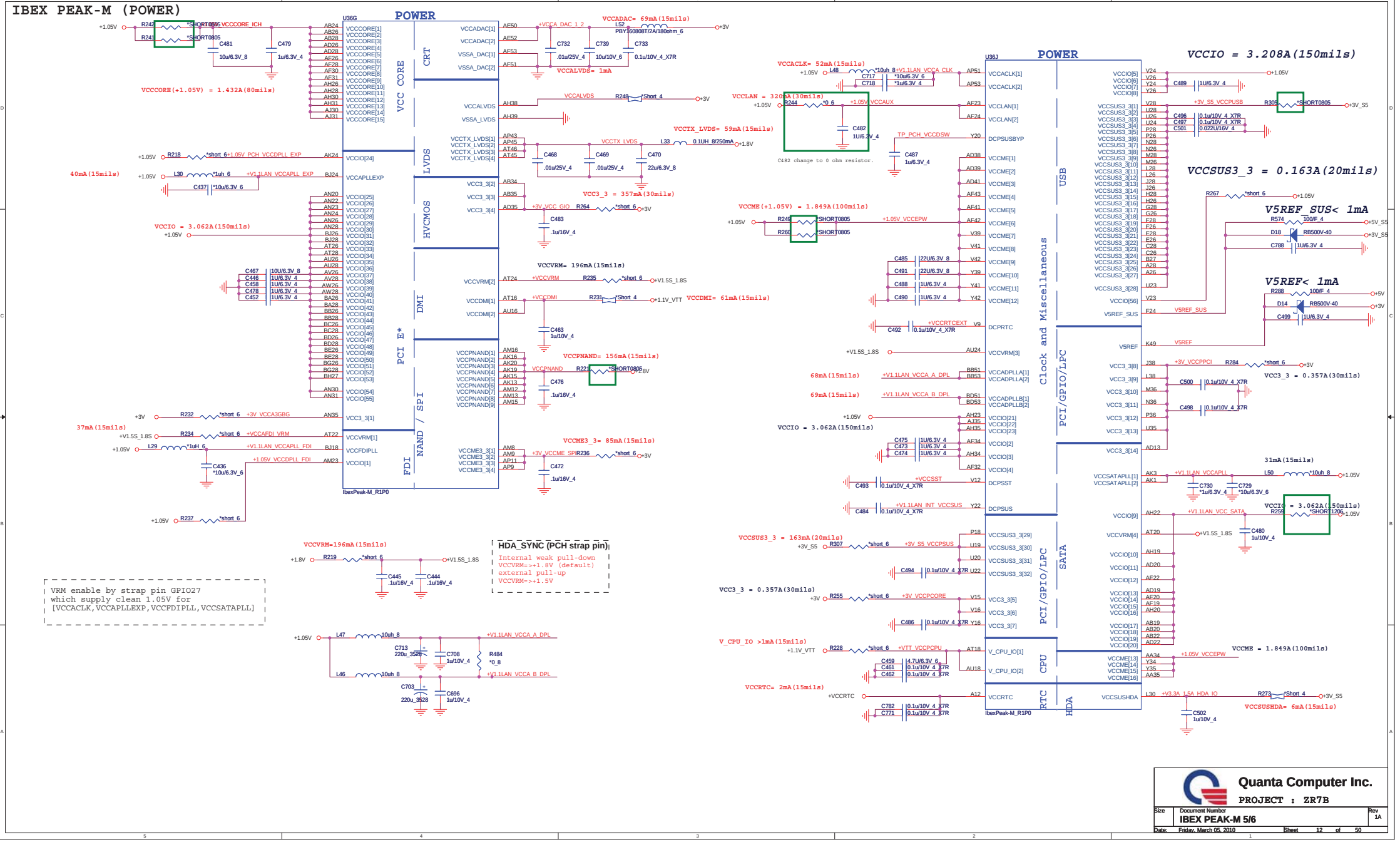
IBEX PEAK-M (POWER)



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	IBEX PEAK-M 5/6	1A

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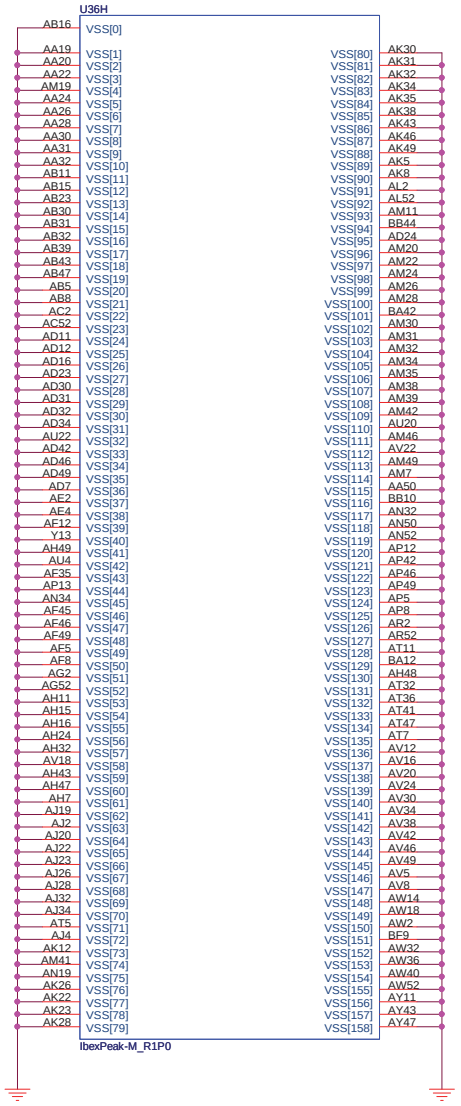
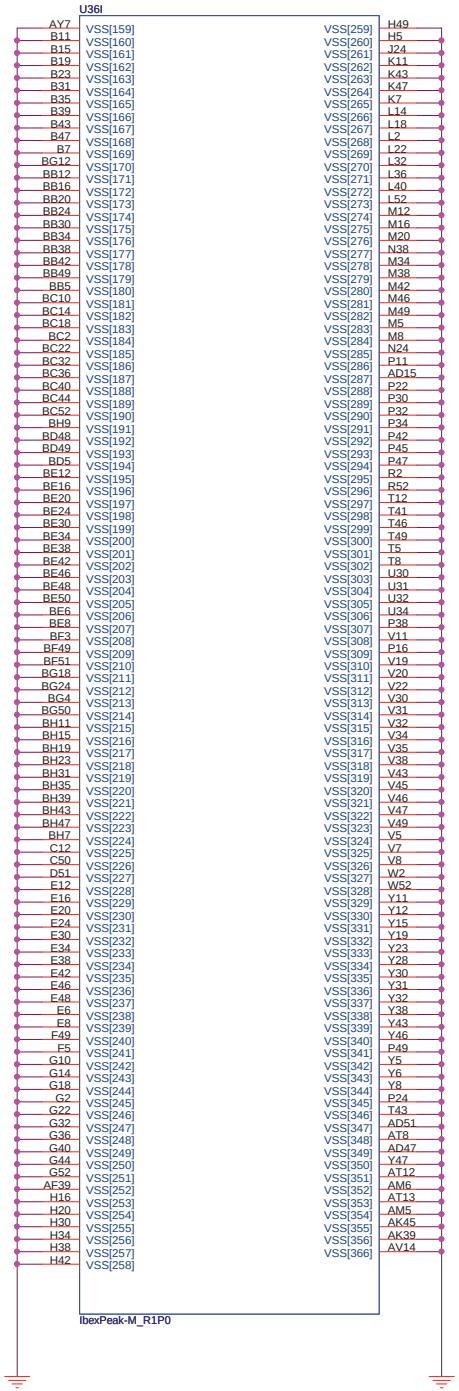
IBEX PEAK-M (GND)



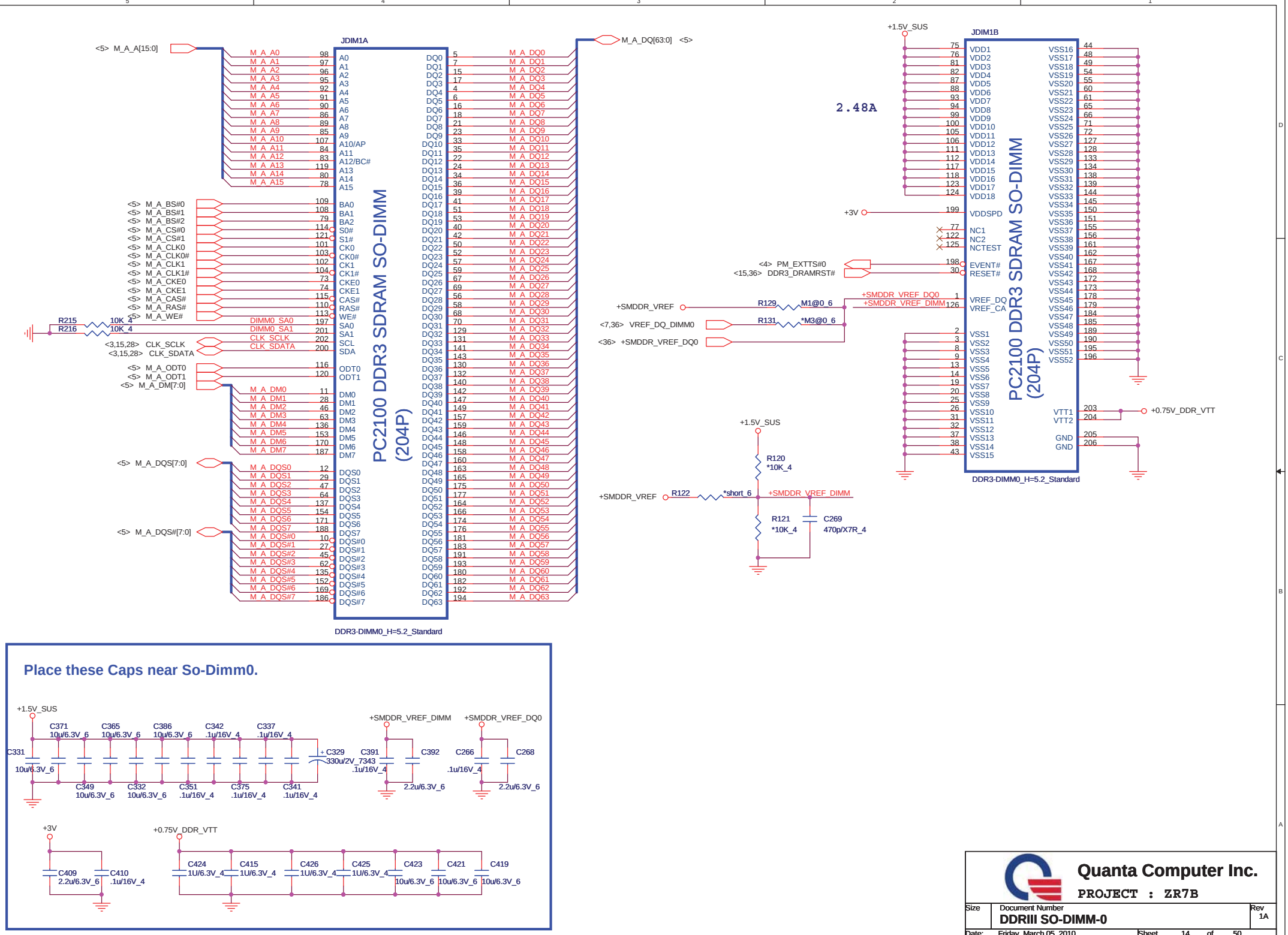


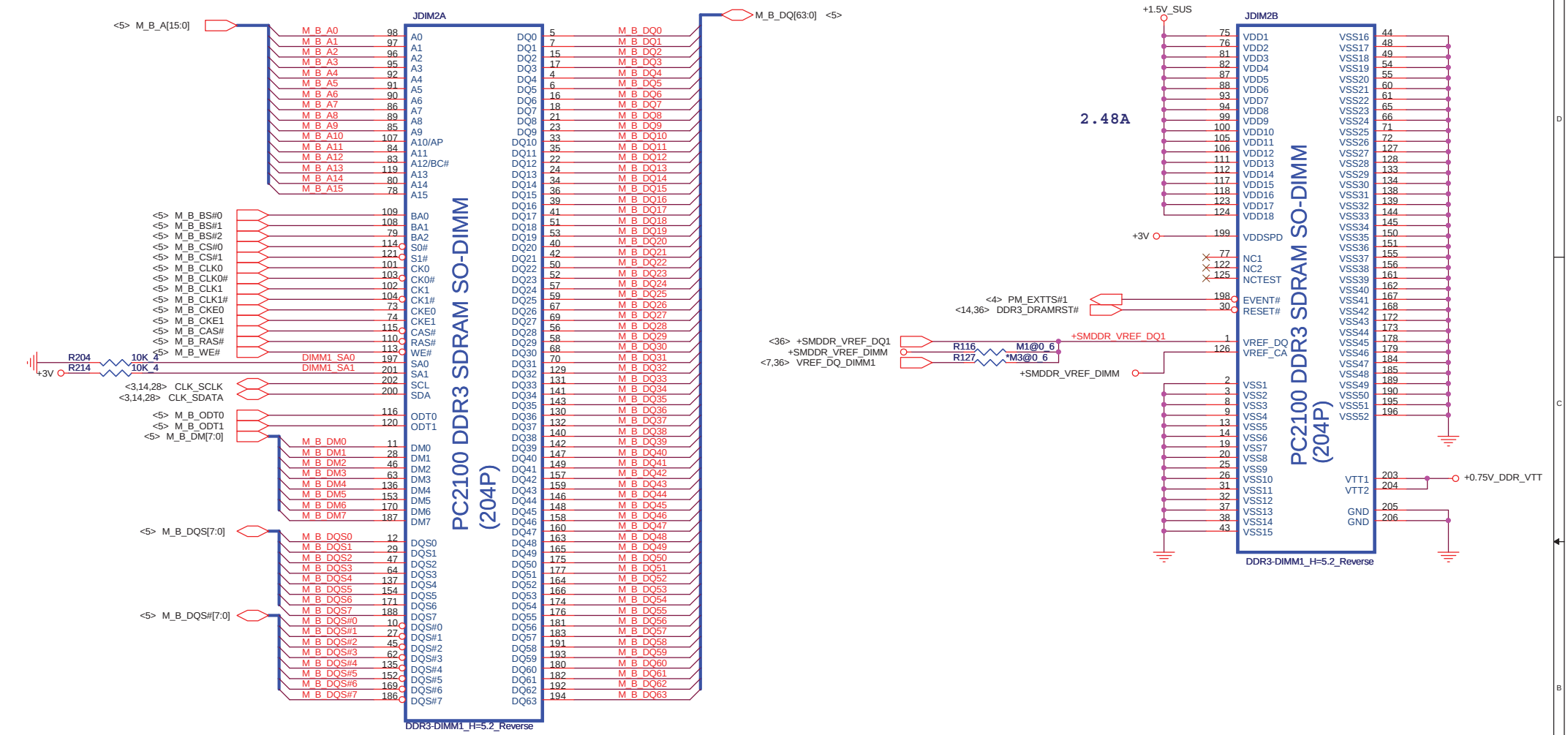
Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

Date: Friday, March 05, 2010 Sheet 13 of 50


JDIM1A
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM0_H=5.2_Standard
<5> M_A_A[15:0]
M_A_DQ[63:0] <5>
<5> M_A_BS#0
<5> M_A_BS#1
<5> M_A_BS#2
<5> M_A_CS#0
<5> M_A_CS#1
<5> M_A_CLK0
<5> M_A_CLK0#
<5> M_A_CLK1
<5> M_A_CLK1#
<5> M_A_CKE0
<5> M_A_CKE1
<5> M_A_CAS#
<5> M_A_RAS#
<5> M_A_WE#
R215 10K_4
R216 10K_4
DIMM0_SA0
DIMM0_SA1
<3,15,28> CLK_SCLK
<3,15,28> CLK_SDATA
<5> M_A_ODT0
<5> M_A_ODT1
<5> M_A_DM[7:0]
<5> M_A_DQS[7:0]
<5> M_A_DQS#[7:0]
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM0_H=5.2_Standard
+1.5V_SUS
2.48A
+3V
<4> PM_EXTTS#0
<15,36> DDR3_DRAMRST#
+SMDDR_VREF
R129 M1@0_6
+SMDDR_VREF_DQ0
+SMDDR_VREF_DIMM
<7,36> VREF_DQ_DIMM0
R131 *M3@0_6
<36> +SMDDR_VREF_DQ0
+0.75V_DDR_VTT
R120 *10K_4
R122 *short_6
R121 *10K_4
C269 470p/X7R_4
Place these Caps near So-Dimm0.
C371 10u/6.3V_6
C365 10u/6.3V_6
C386 10u/6.3V_6
C342 .1u/16V_4
C337 .1u/16V_4
C331 10u/6.3V_6
C329 330u/2V_7343
C349 10u/6.3V_6
C332 10u/6.3V_6
C351 .1u/16V_4
C375 .1u/16V_4
C341 .1u/16V_4
+SMDDR_VREF_DIMM
+SMDDR_VREF_DQ0
C391 .1u/16V_4
C392 2.2u/6.3V_6
C266 .1u/16V_4
C268 2.2u/6.3V_6
C409 2.2u/6.3V_6
C410 .1u/16V_4
C424 1U/6.3V_4
C415 1U/6.3V_4
C426 1U/6.3V_4
C425 1U/6.3V_4
C423 10u/6.3V_6
C421 10u/6.3V_6
C419 10u/6.3V_6
Quanta Computer Inc.
PROJECT : ZR7B
Size
Document Number
DDRIII SO-DIMM-0
Rev 1A
Date: Friday, March 05, 2010
Sheet 14 of 50

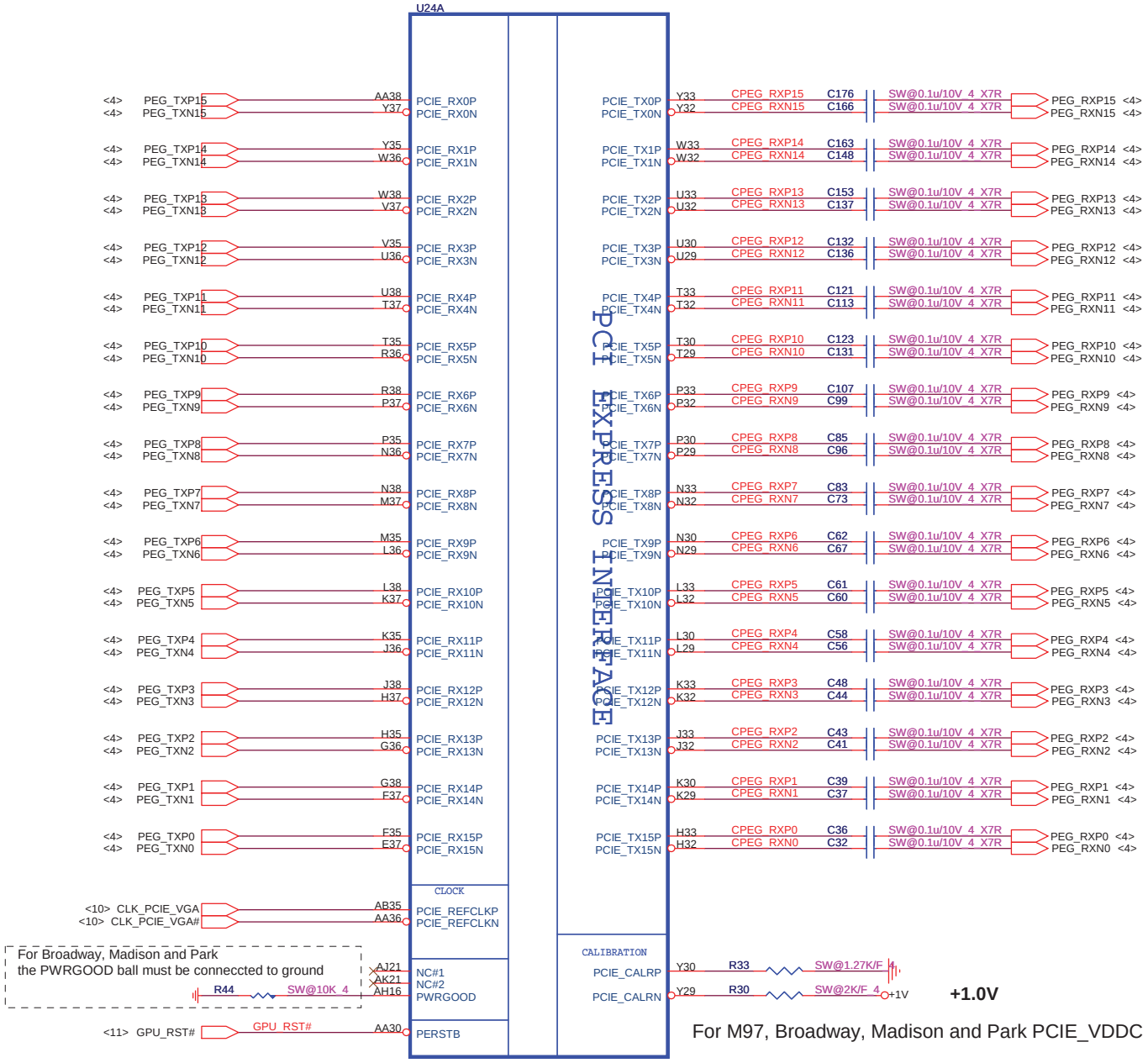


Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

Date: Friday, March 05, 2010 Sheet 15 of 50



For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Quanta Computer Inc.

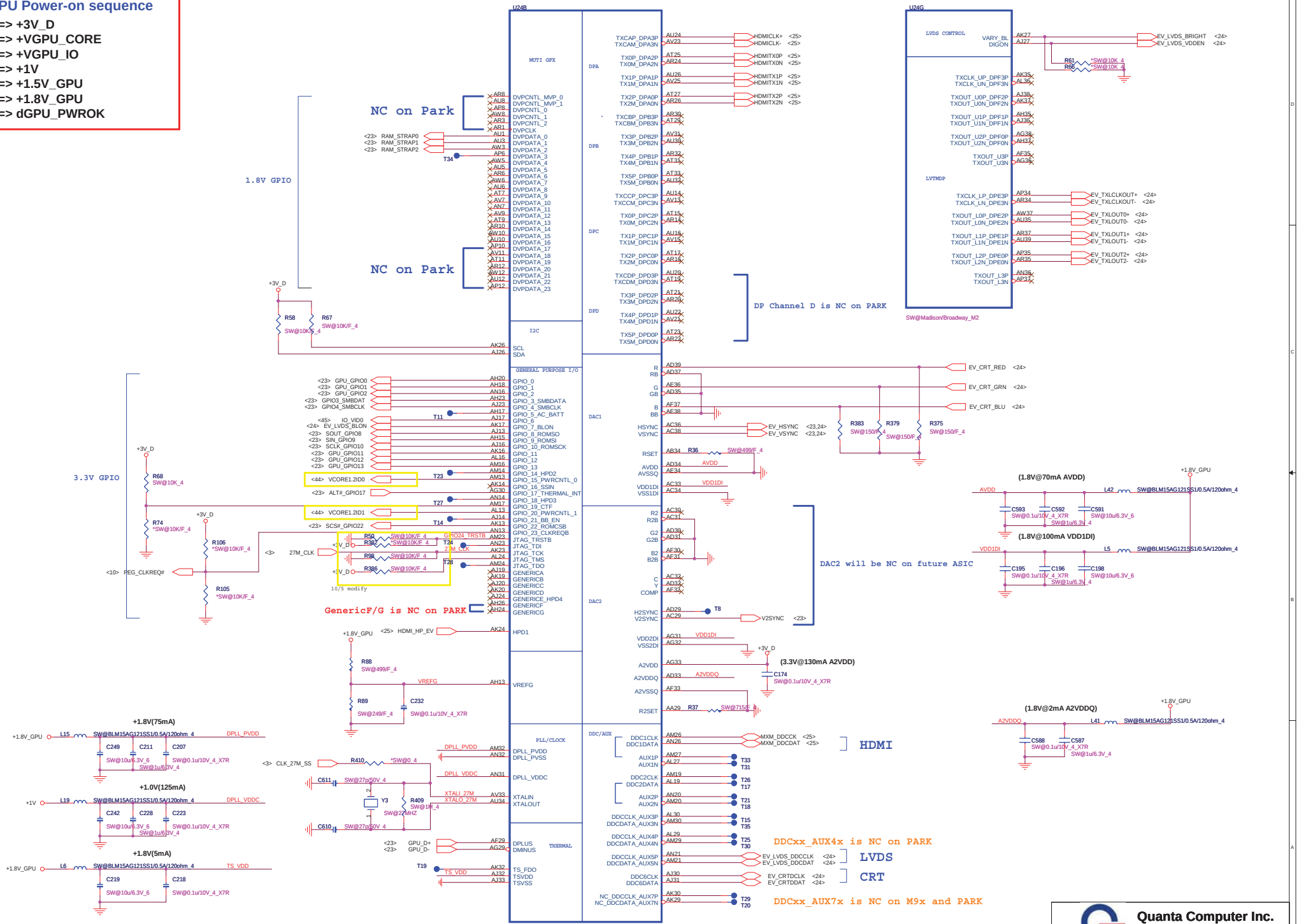
PROJECT : ZR7B

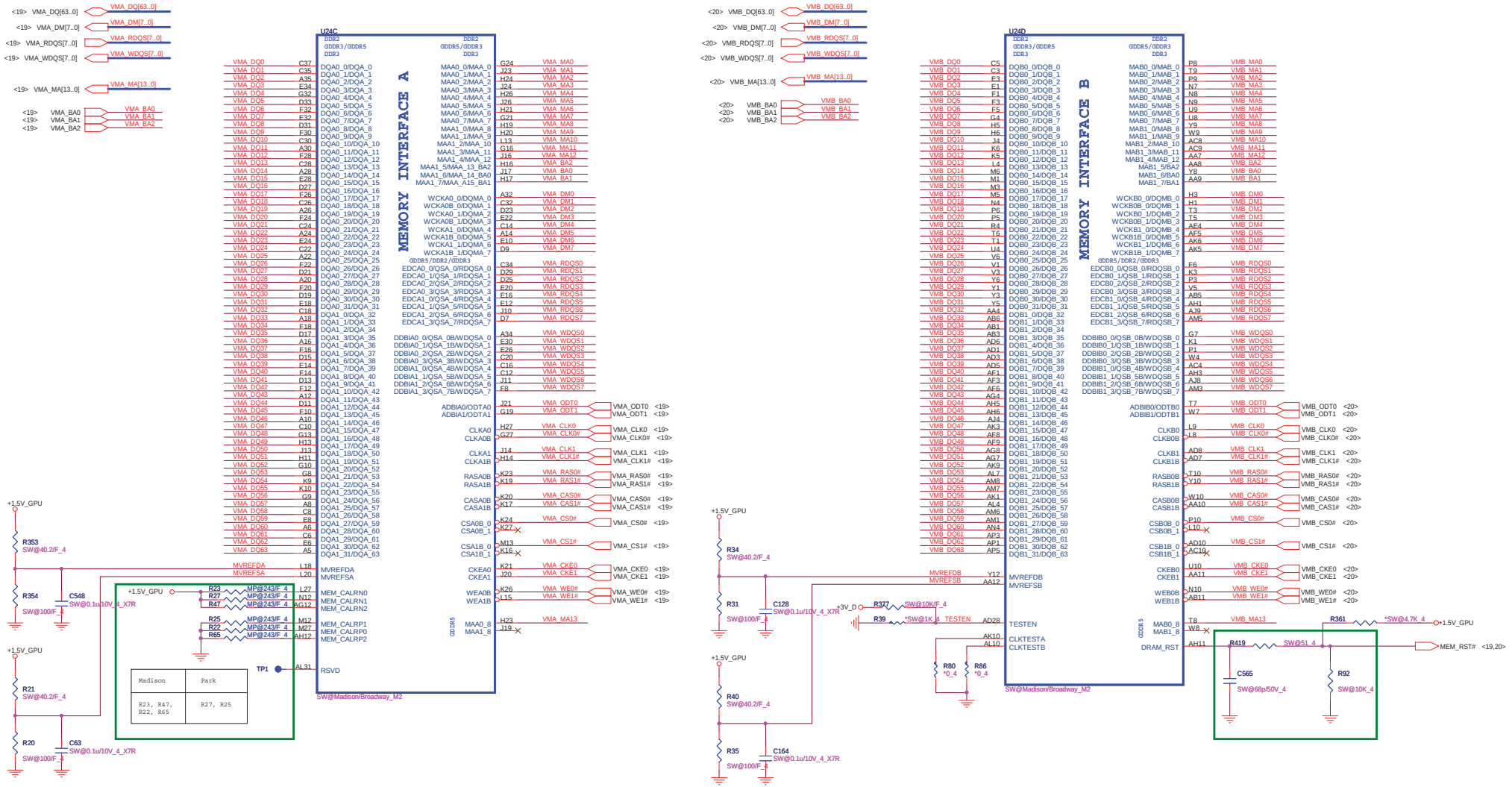
Size	Document Number	Rev
	Madison/Broadway-PCIE I/F	1A

Date: Friday, March 05, 2010 Sheet 16 of 50

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK





Quanta Computer Inc.

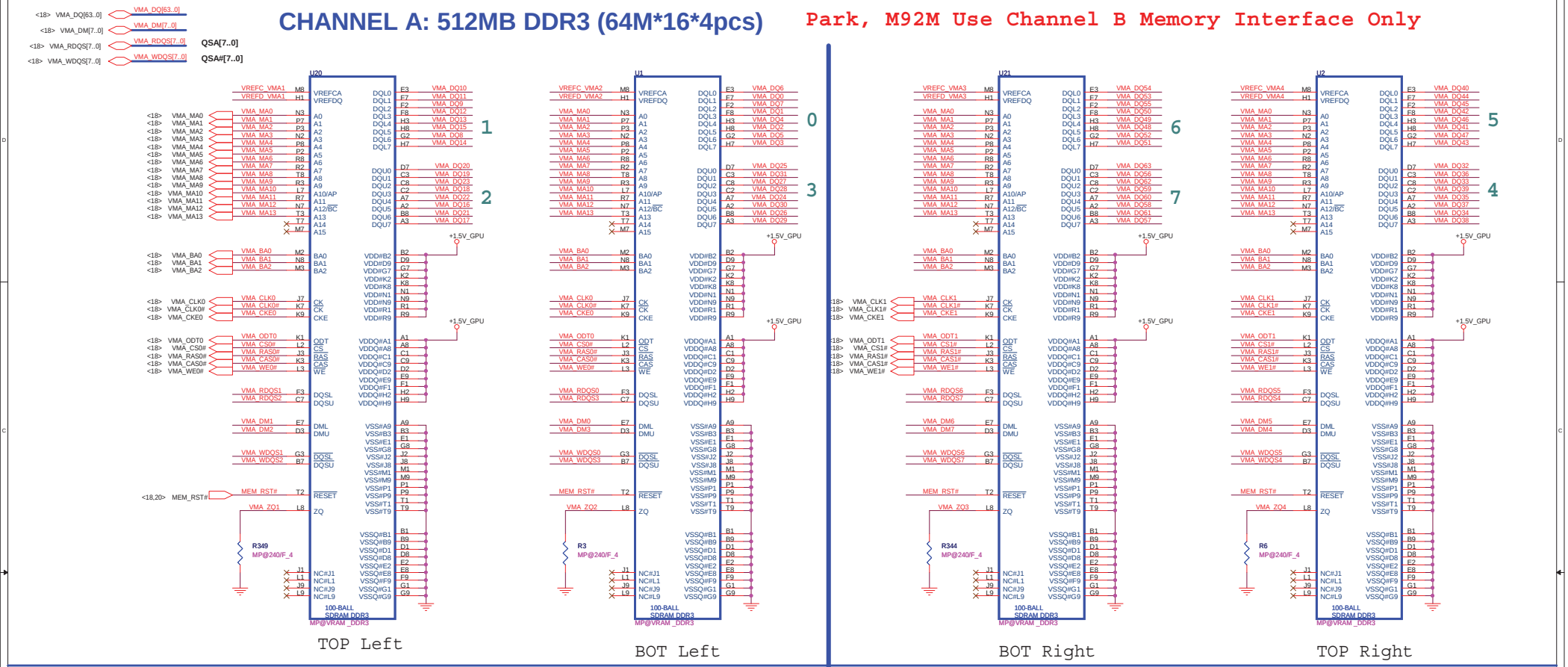
PROJECT : ZR7B

Size	Document Number	Rev
	Madison/Broadway-MEM I/F	1A

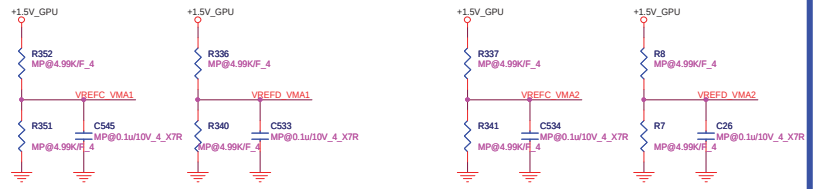
Date: Friday, March 05, 2010 Sheet 18 of 50

CHANNEL A: 512MB DDR3 (64M*16*4pcs)

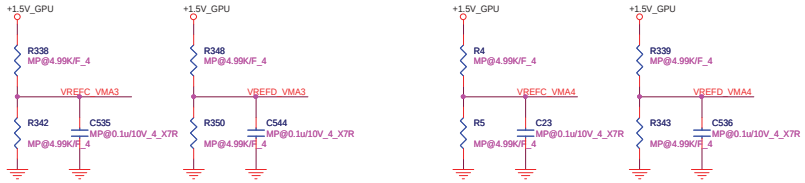
Park, M92M Use Channel B Memory Interface Only



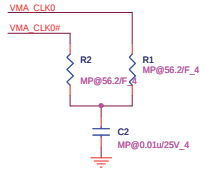
Group-A0 VREF



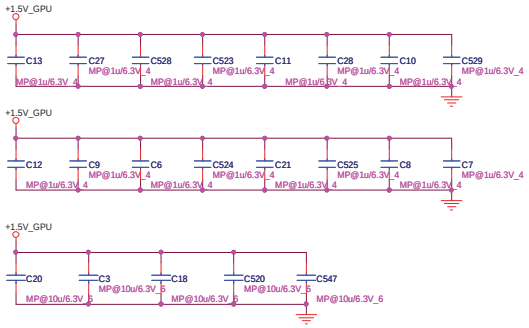
Group-A1 VREF



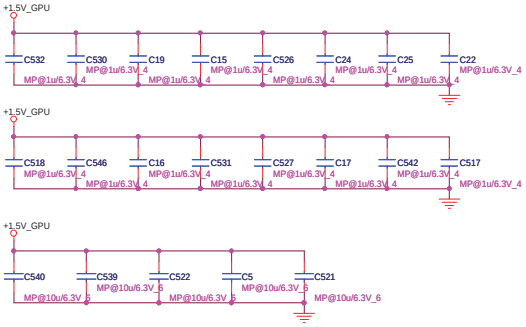
MEM_A0 CLK



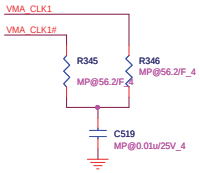
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	MEMORY 1 channel A	1A

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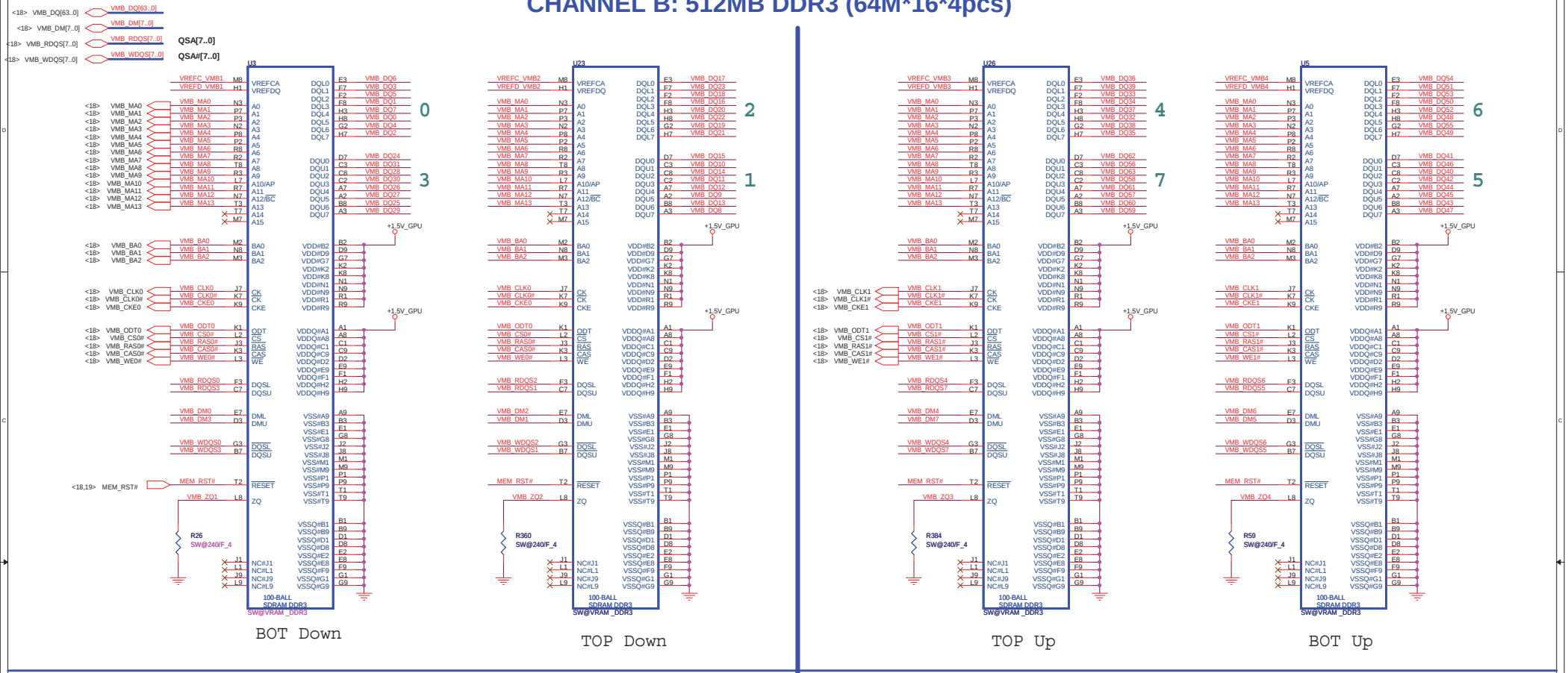
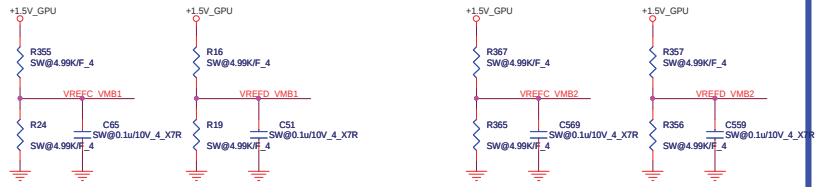
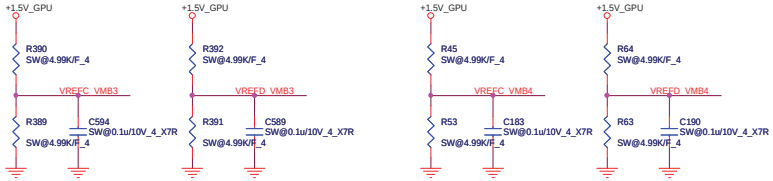
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



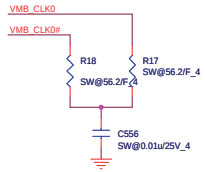
Group-B0 VREF



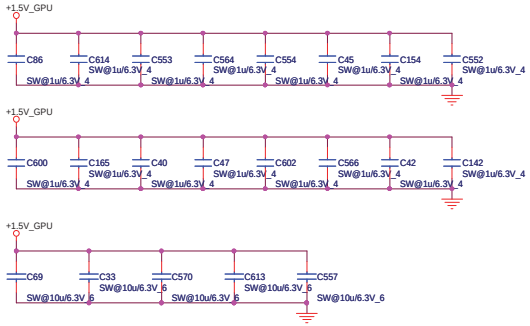
Group-B1 VREF



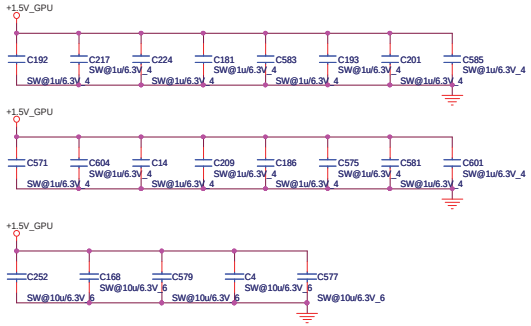
MEM_B0 CLK



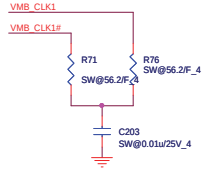
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	MEMORY 2 channel B	1A

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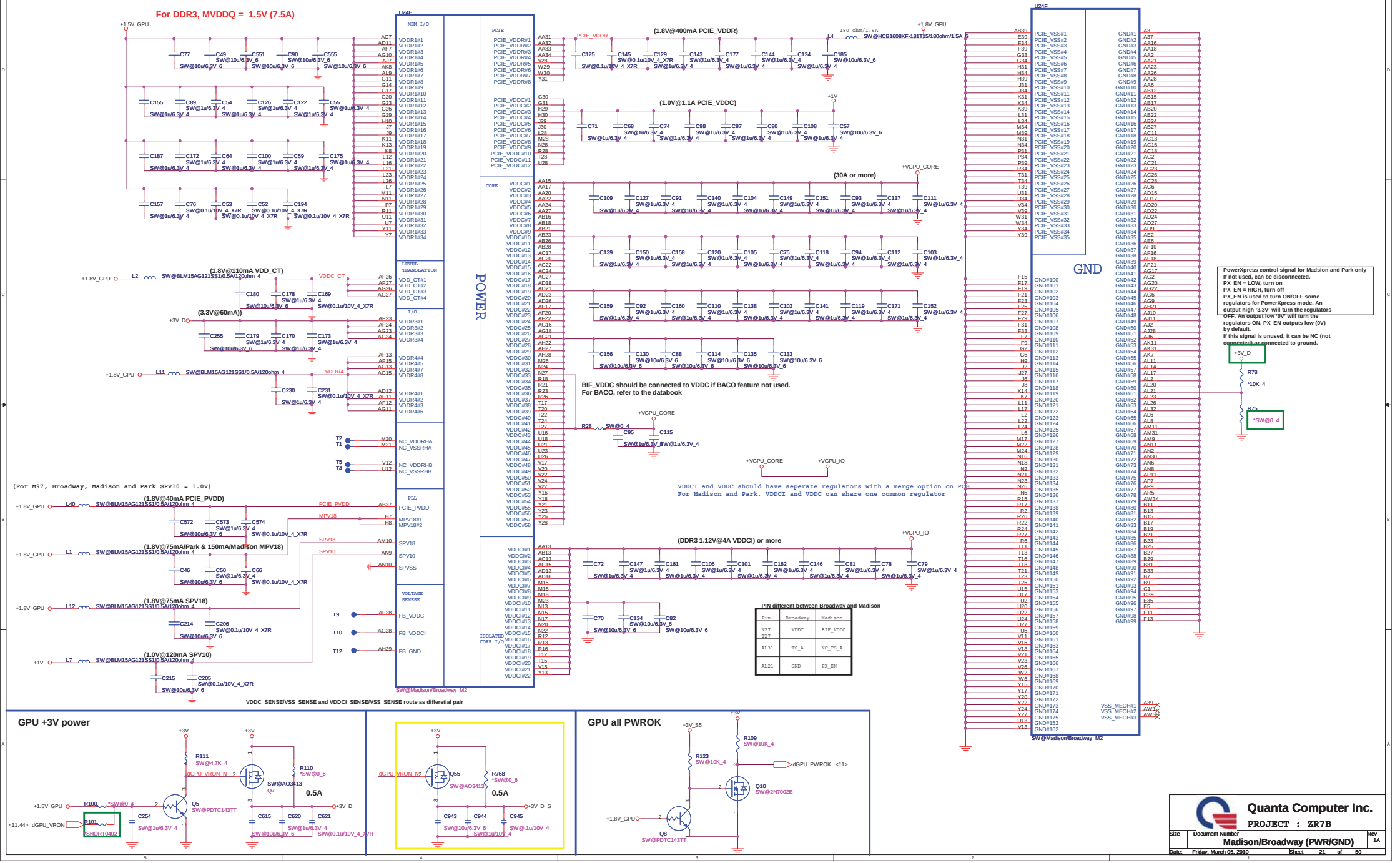
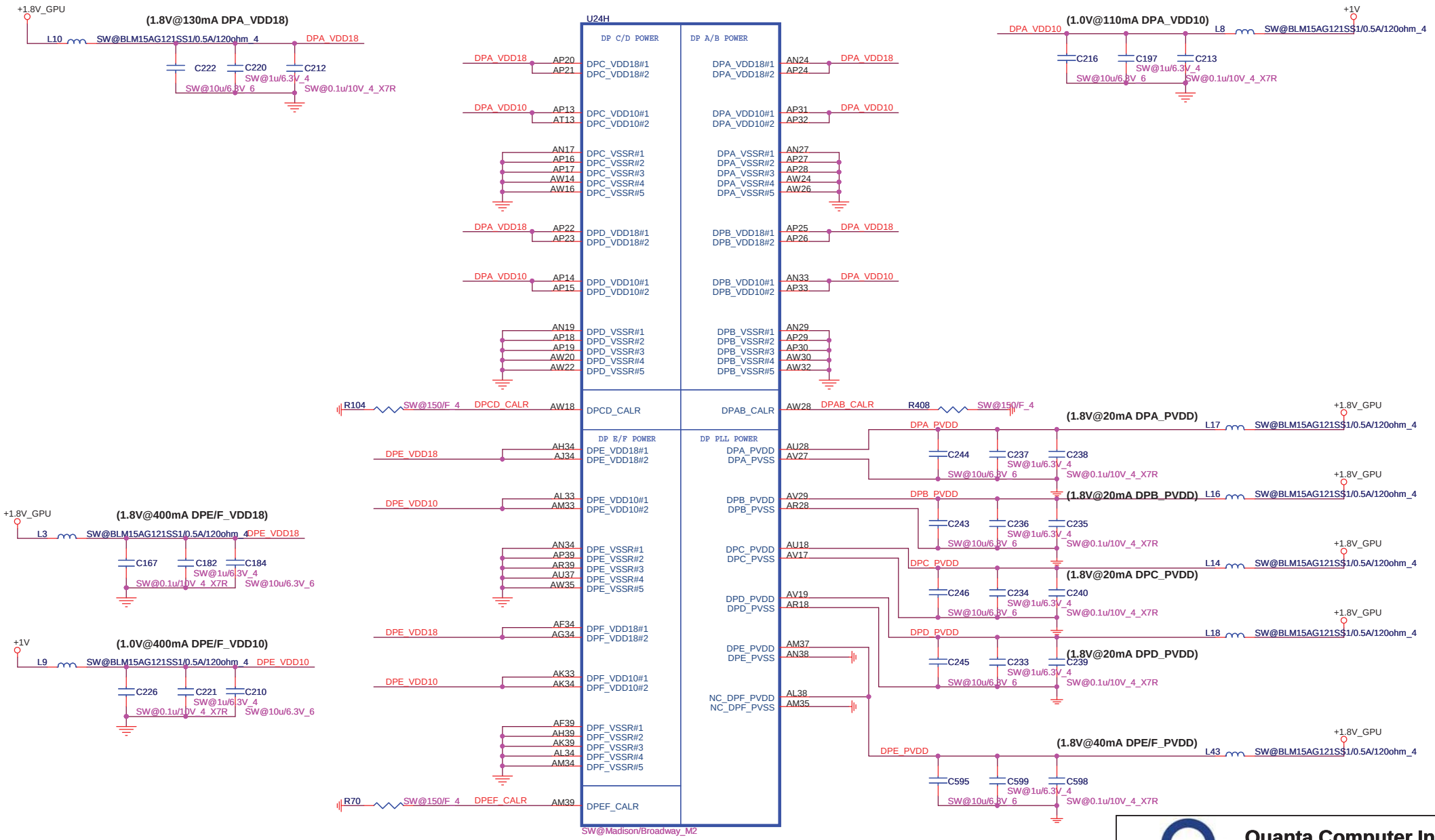


PIN different between Broadway and Madison

Pin	Broadway	Madison
N27 T27	VDDC	BIF_VDDC
AL31	TS_A	NC_TS_A
AL21	GND	PX_EN



Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	Madison/Broadway (DP_PWR/GND)	1A

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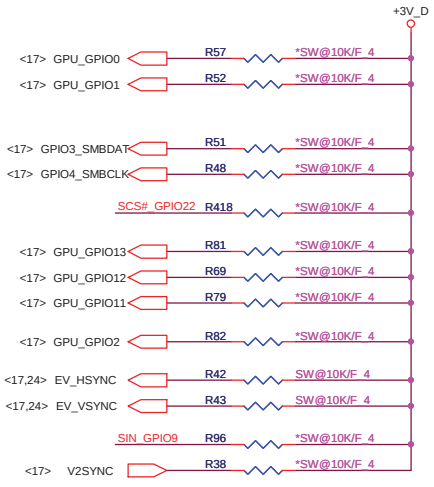
PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

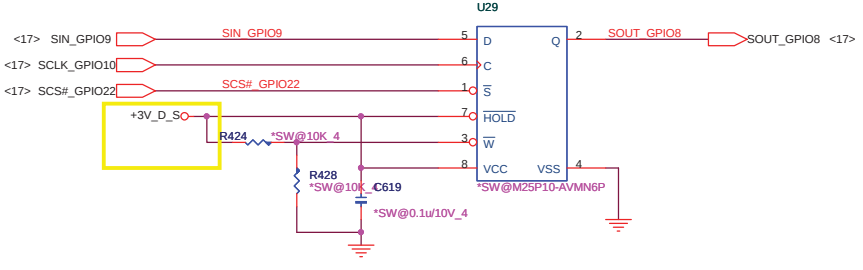
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

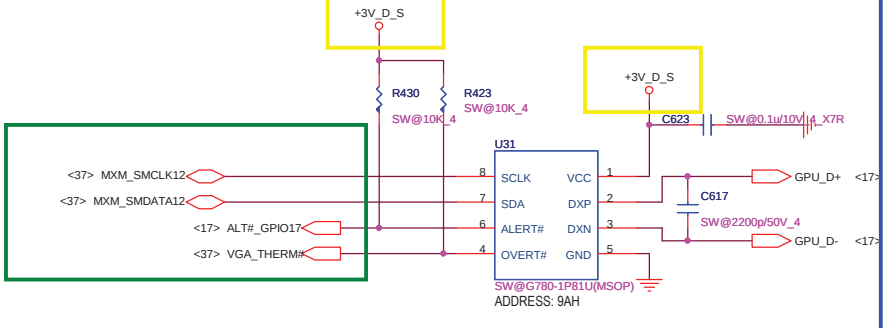
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM



Thermal Sensor

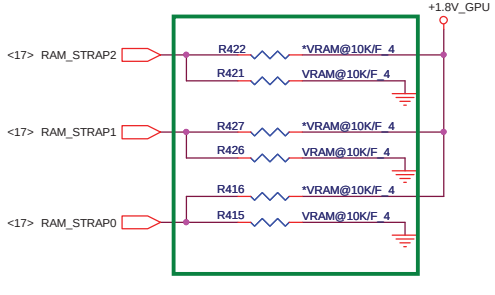
NS	none
WINDBOND	AL83L771K02
GMT	AL000780003



DDR3 Memory Aperture size

DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB	1	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	512MB			
			1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	1GB	0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	Strip/Thermal	1A

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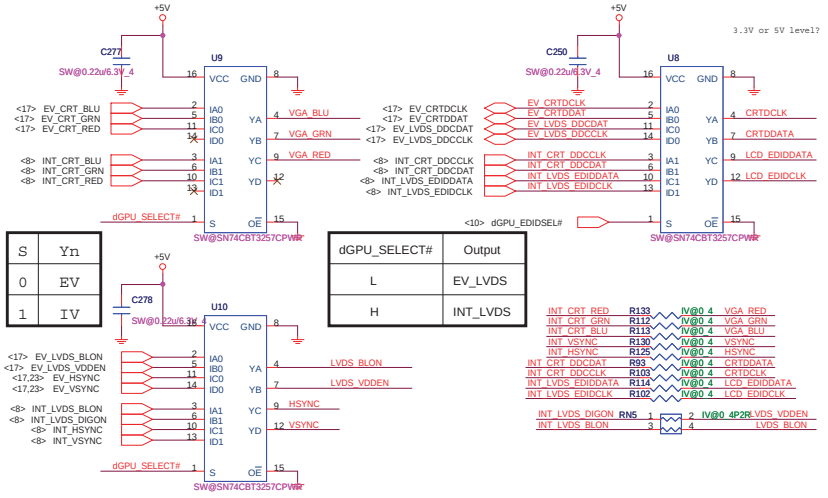
CRT Switch

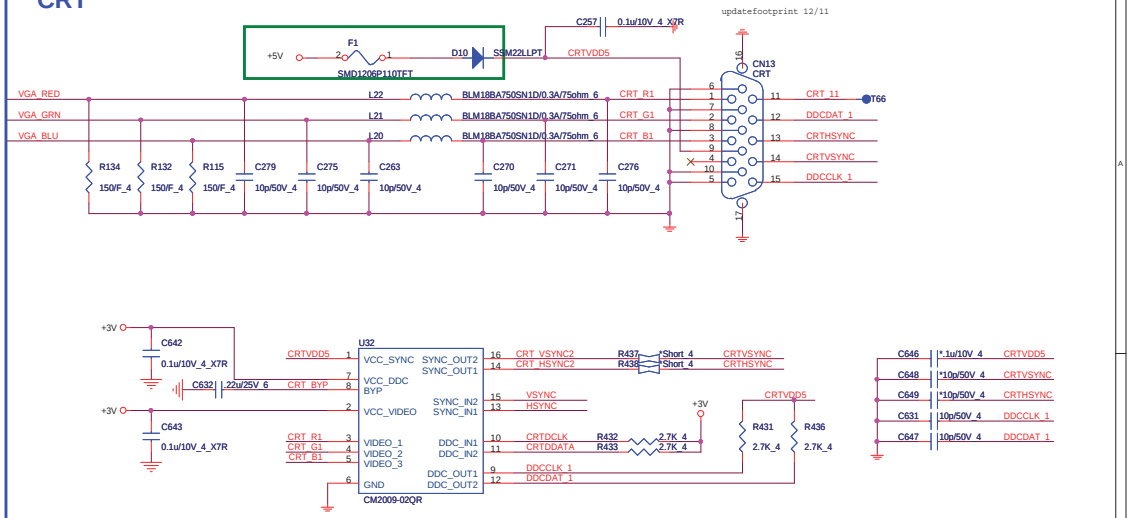
IV@
SW@



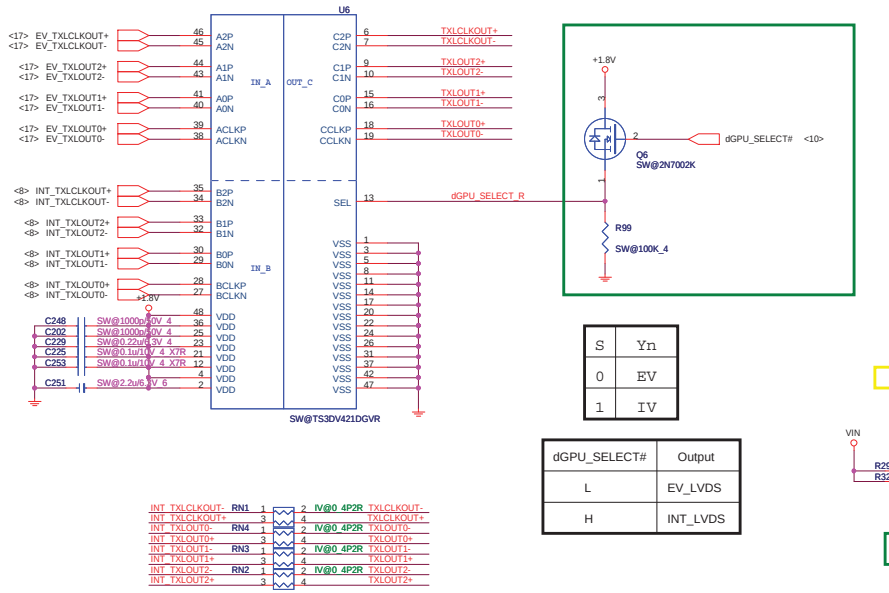
S	Yn
0	EV
1	IV

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

CRT



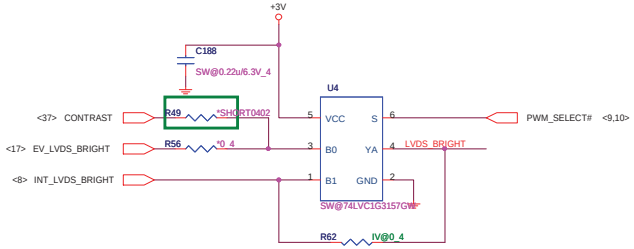
LVDS Switch

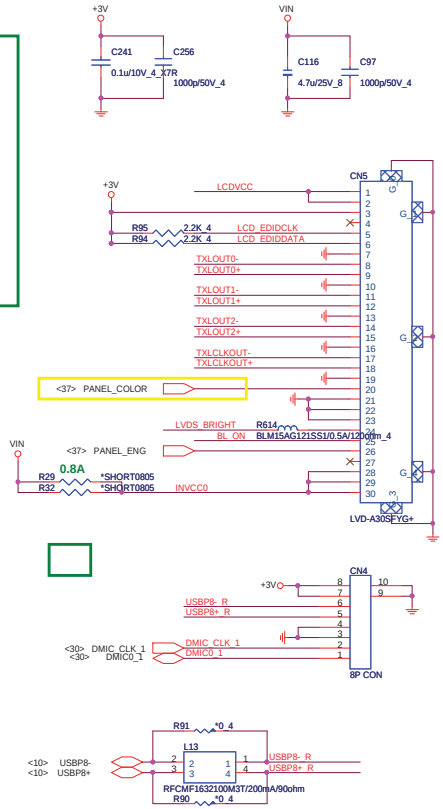


LVDS

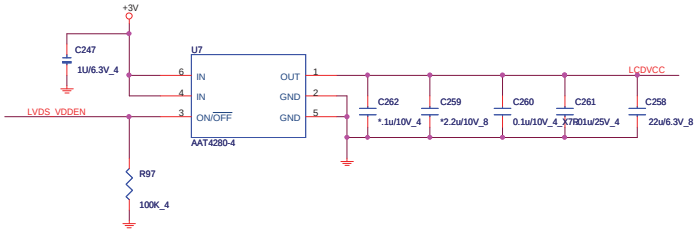
S	Yn
0	EV
1	IV

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

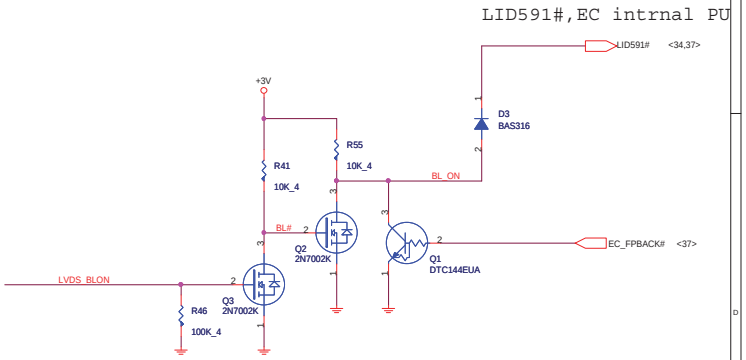




LCD Power



Backlight Control



Quanta Computer Inc.

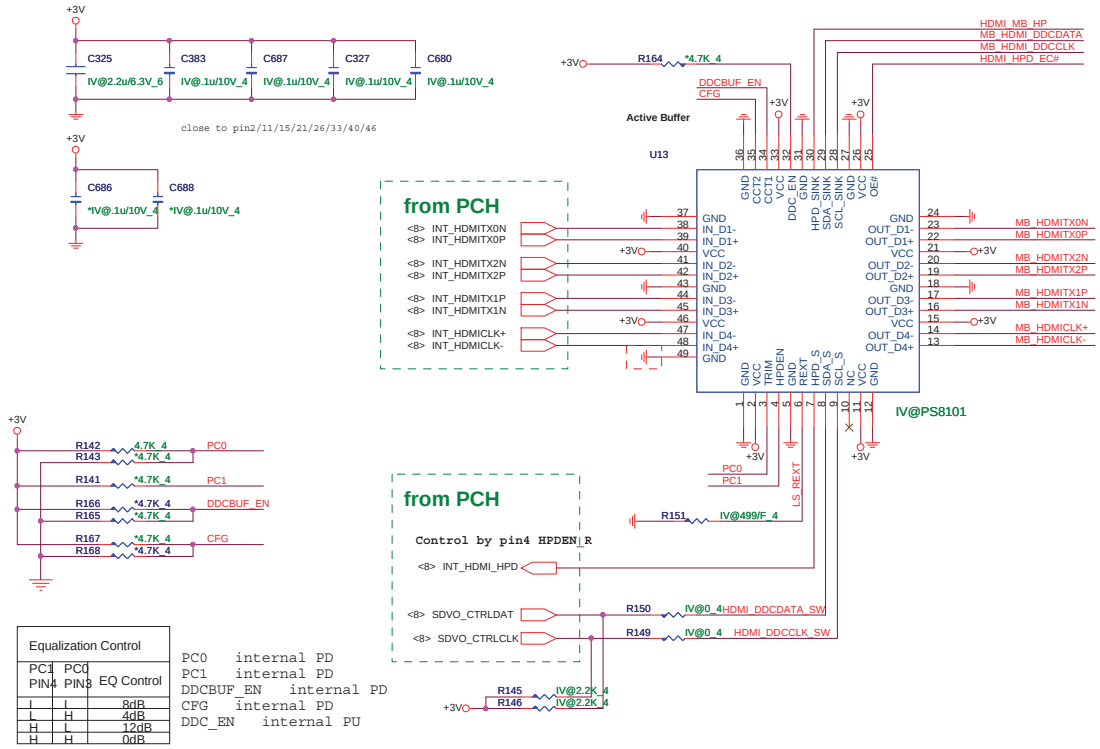
PROJECT : ZR7B

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A

Date: Friday, March 05, 2010 Sheet 24 of 50

I@ HDMI LEVEL SHIFTER

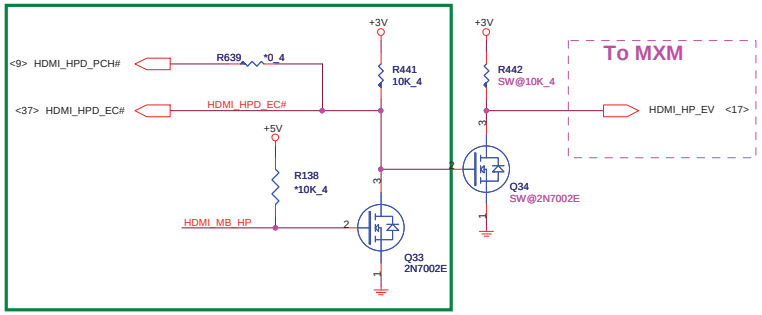
IV@
SW@
SP@



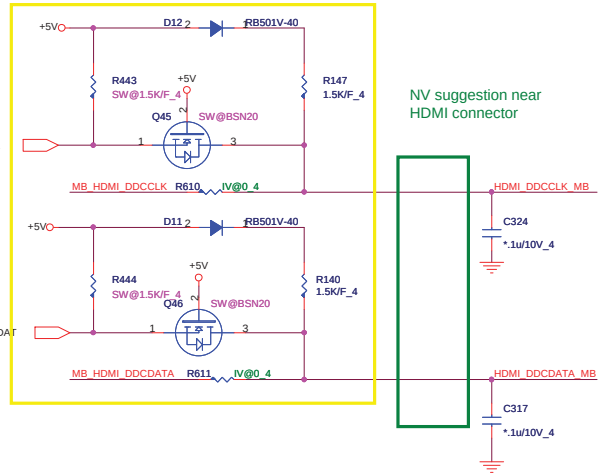
Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

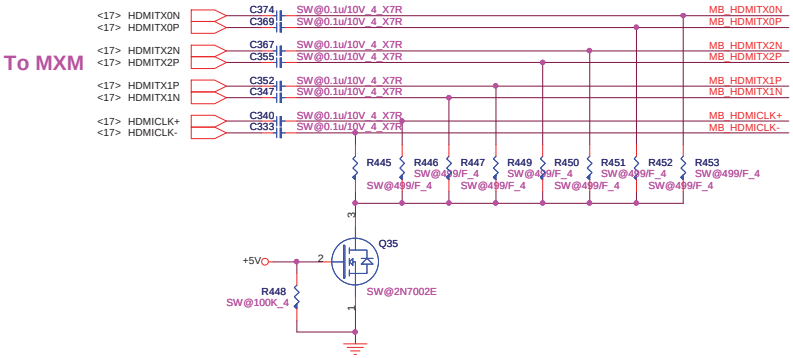
SW@HDMI-detect



I2C

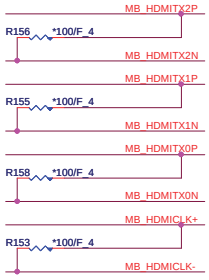


Switchable Graphic HDMI source

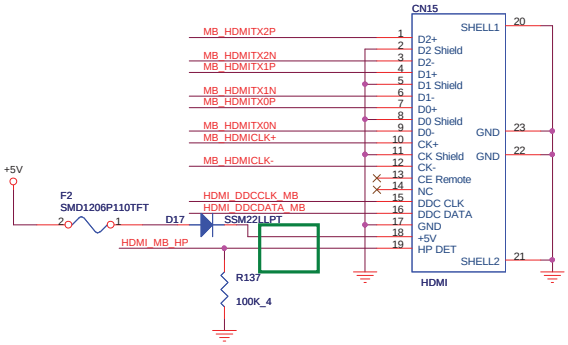


ESD Protect

EMI

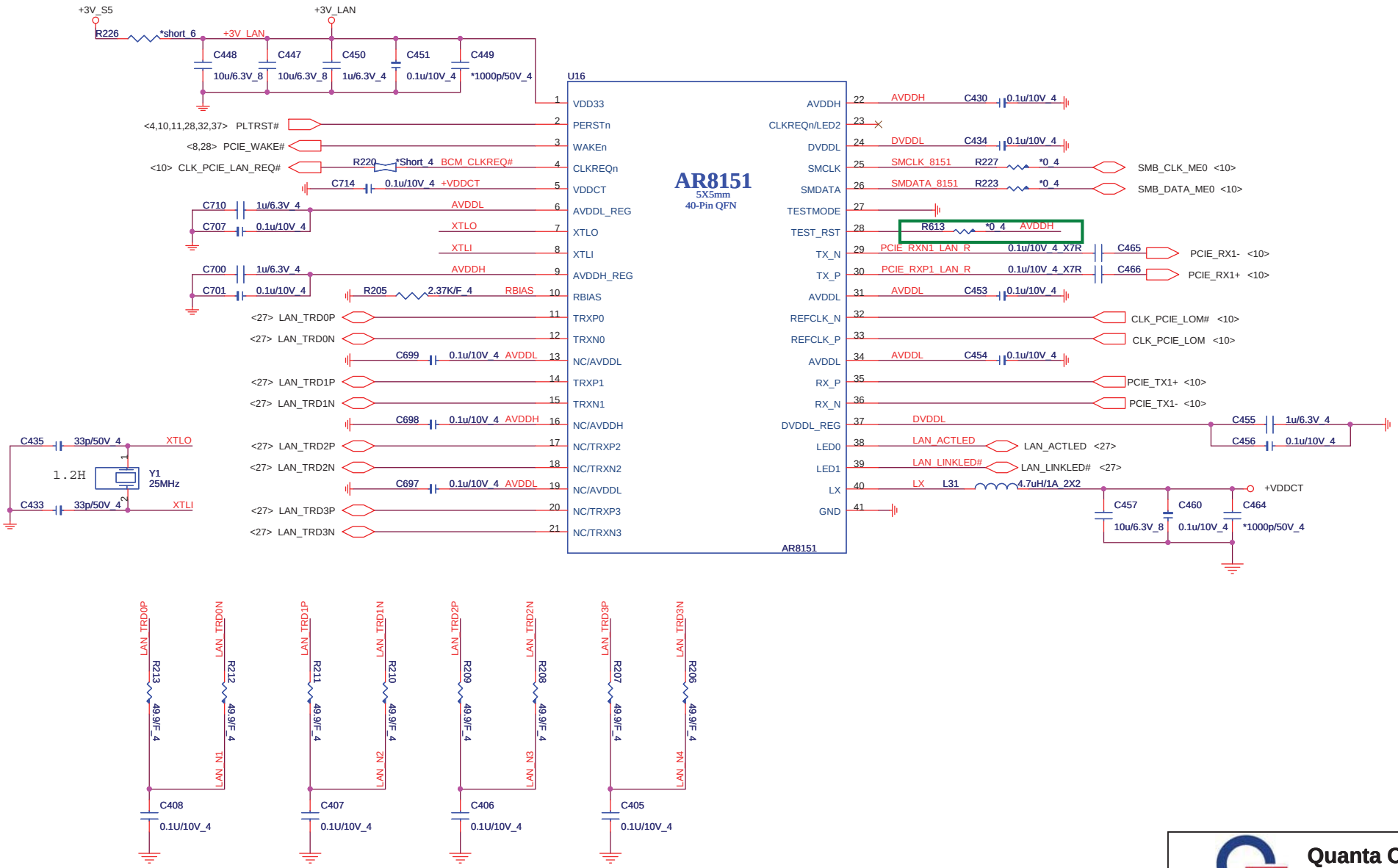


HDMI connector



Quanta Computer Inc.		
PROJECT : ZR7B		
Size	Document Number	Rev
	HDMI (PS8101)	1A
Date: Friday, March 05, 2010	Sheet 25 of 50	

Giga-LAN AR8151

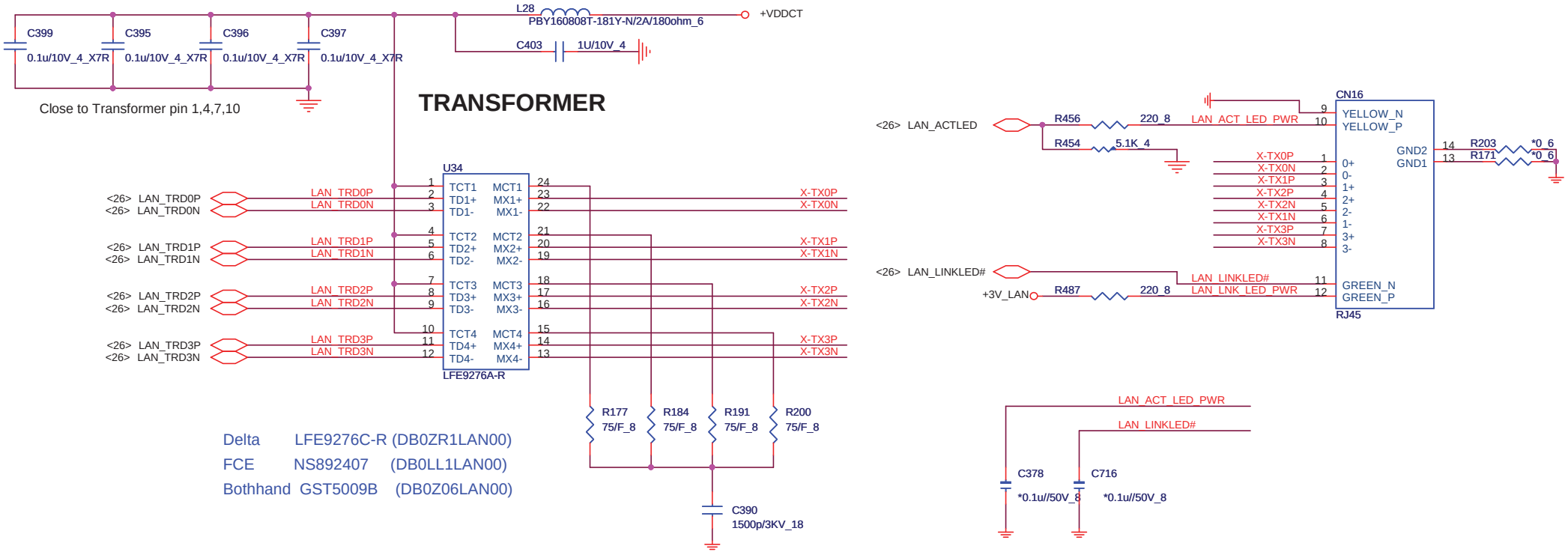


Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	GLAN BCM57780	1A

Date: Friday, March 05, 2010 Sheet 26 of 50



Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	LAN Transformer and RJ45	1A

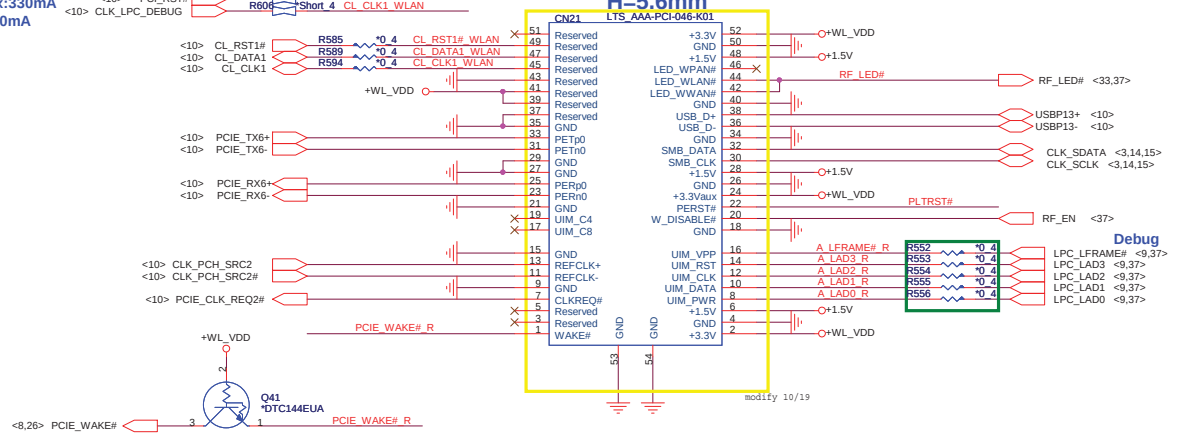
Date: Friday, March 05, 2010 Sheet 27 of 50

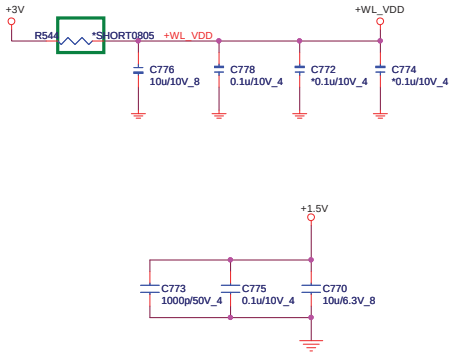
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)

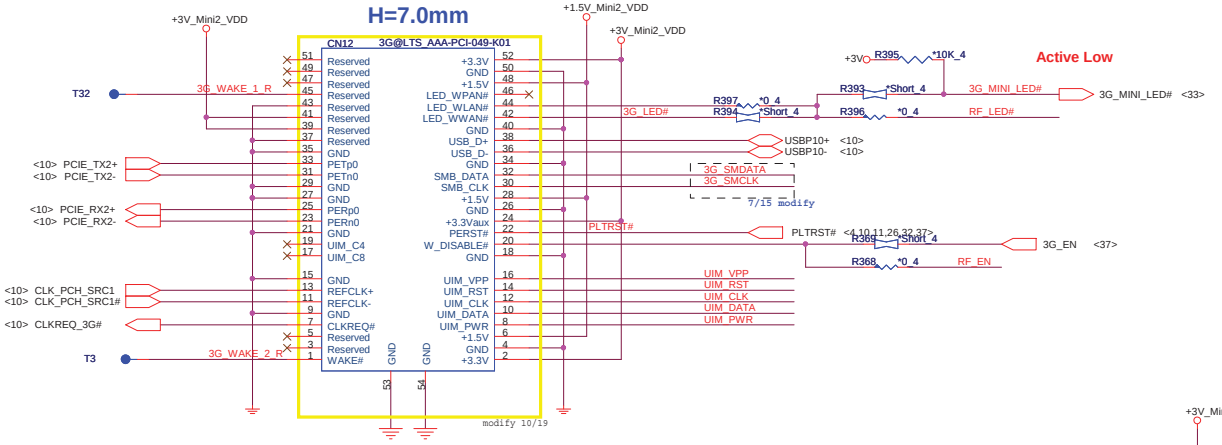
H=5.6mm

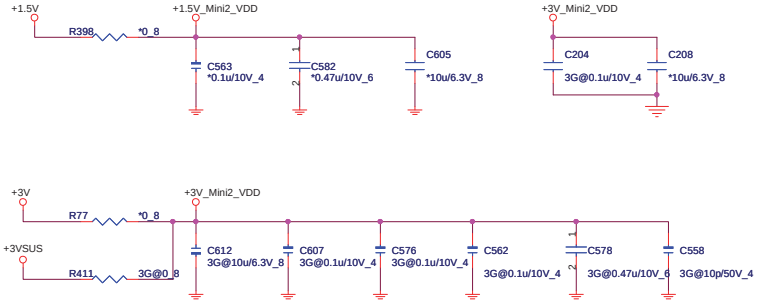




MINI-CARD 3G(MNC)Reserve for JV41-CP

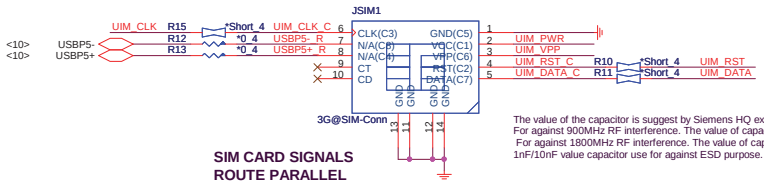
H=7.0mm





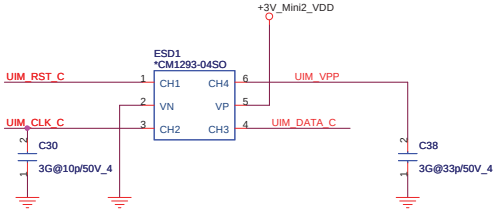
A:(10/17)FAE confirm:
3G module need +3VSUS and no need +1.5V and no need SMBUS

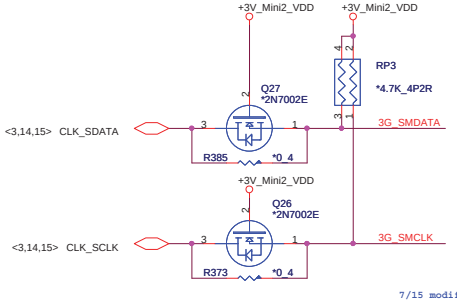
SIM CARD(RFM)Reserve for JV41-CP

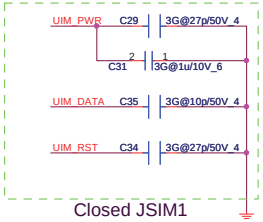


SIM CARD SIGNALS
ROUTE PARALLEL

The value of the capacitor is suggest by Siemens HQ expert.
For against 900MHz RF interference. The value of capacitor is 27pF.
For against 1800MHz RF interference. The value of capacitor is 10pF.
1nF/10nF value capacitor use for against ESD purpose.







Closed JSIM1

Quanta Computer Inc.		
PROJECT : ZR7B		
Size	Document Number: MINI PCI-E card/TV	Rev 1A
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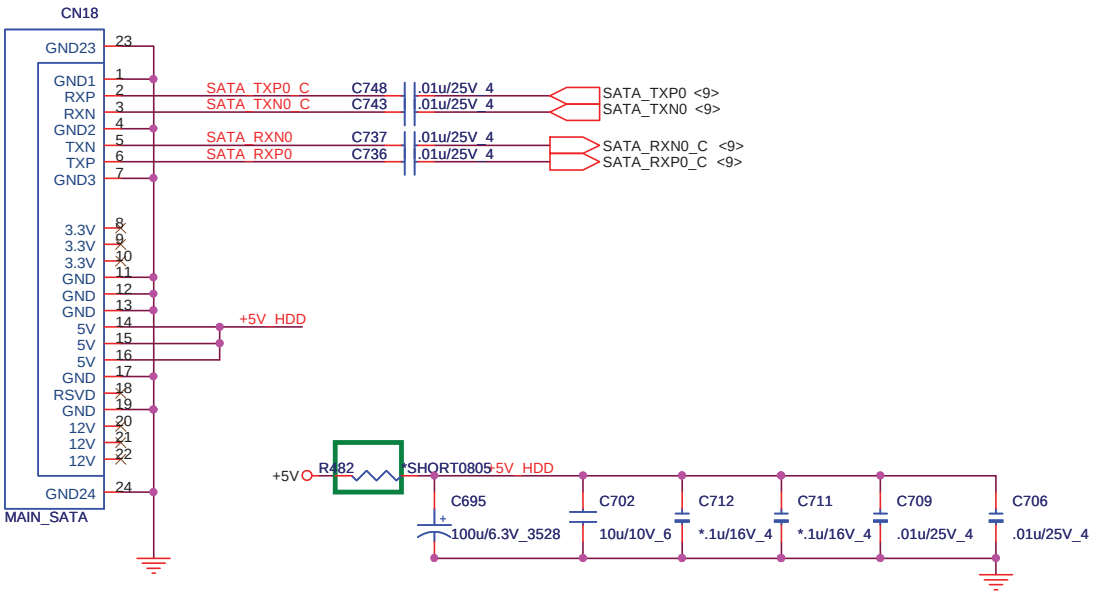
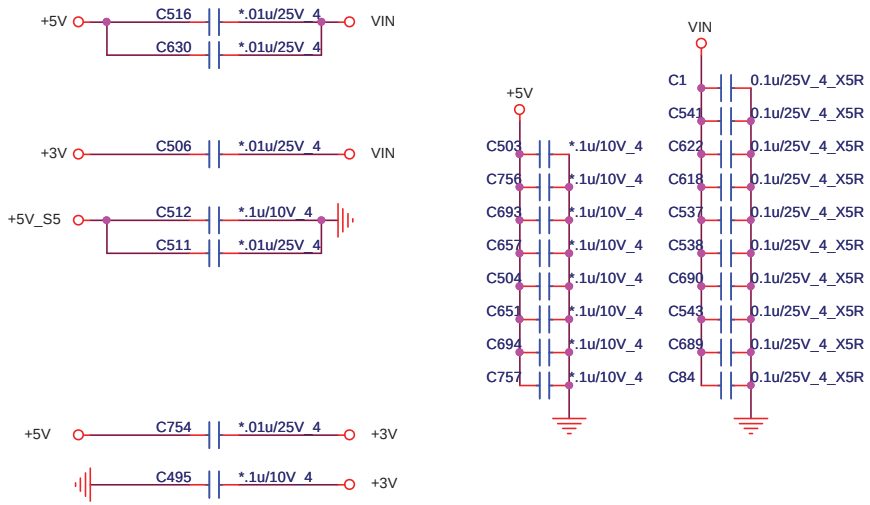
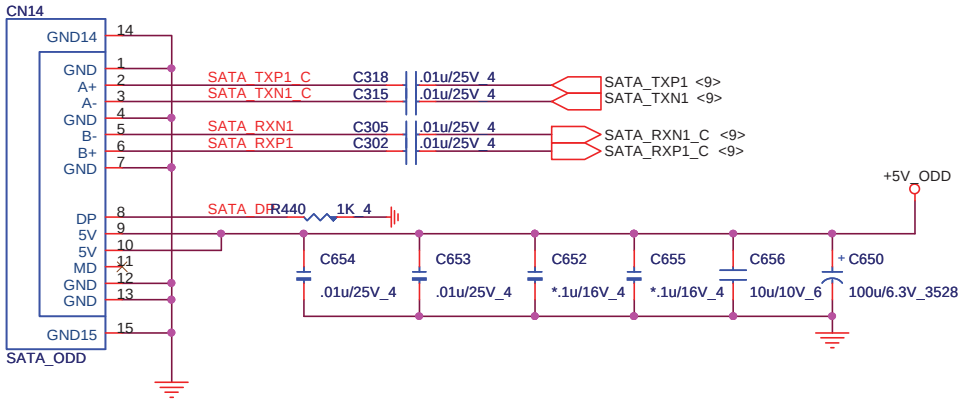
MAIN SATA HDD



EE RETURN-PATH CAPACITORS

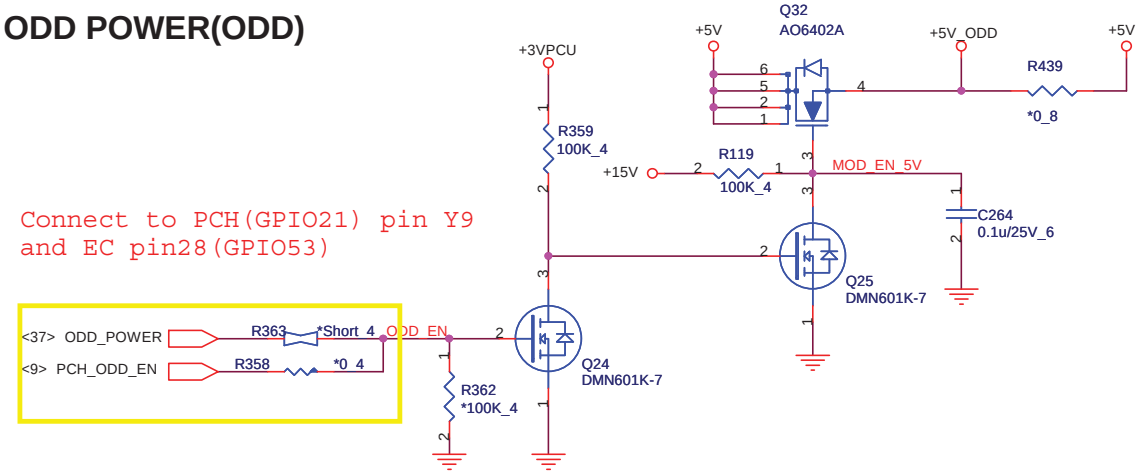


ODD (SATA)



ODD POWER(ODD)

Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)

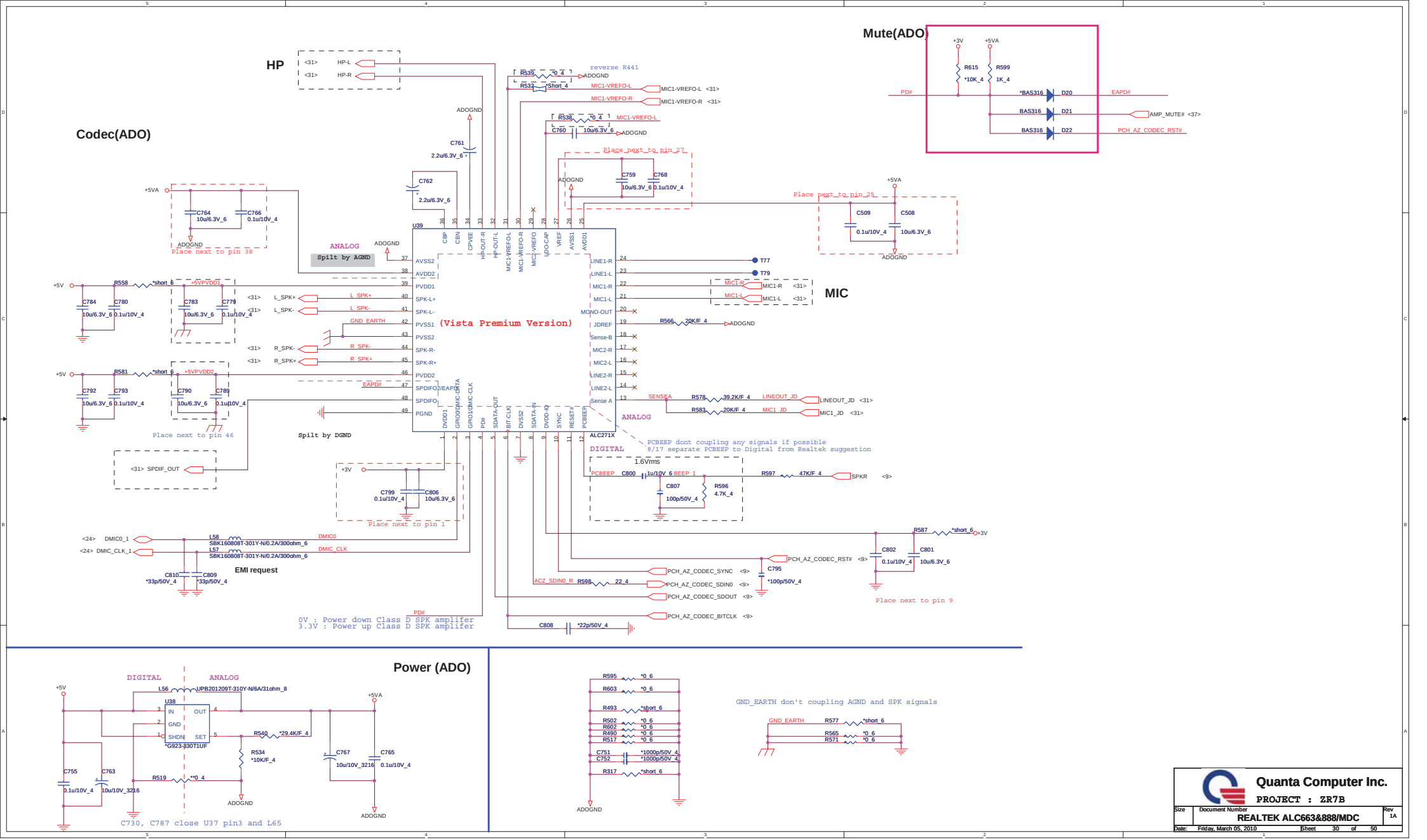


Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A

Date: Friday, March 05, 2010 Sheet 29 of 50


Codec(ADO)
HP
Mute(ADO)
MIC
Power (ADO)
U39
ALC271X
(Vista Premium Version)
ANALOG
DIGITAL
Spilt by AGND
Spilt by DGND
EMI request
Place next to pin 38
Place next to pin 46
Place next to pin 1
Place next to pin 25
Place next to pin 27
Place next to pin 9
reverse R441
PCBEEP dont coupling any signals if possible
8/17 separate PCBEEP to Digital from Realtek suggestion
0V : Power down Class D SPK amplifer
3.3V : Power up Class D SPK amplifer
GND_EARTH don't coupling AGND and SPK signals
C730, C787 close U37 pin3 and L65
U38
*G923-330T1UF
Quanta Computer Inc.
PROJECT : ZR7B
Size
Document Number
REALTEK ALC663&888/MDC
Rev
1A
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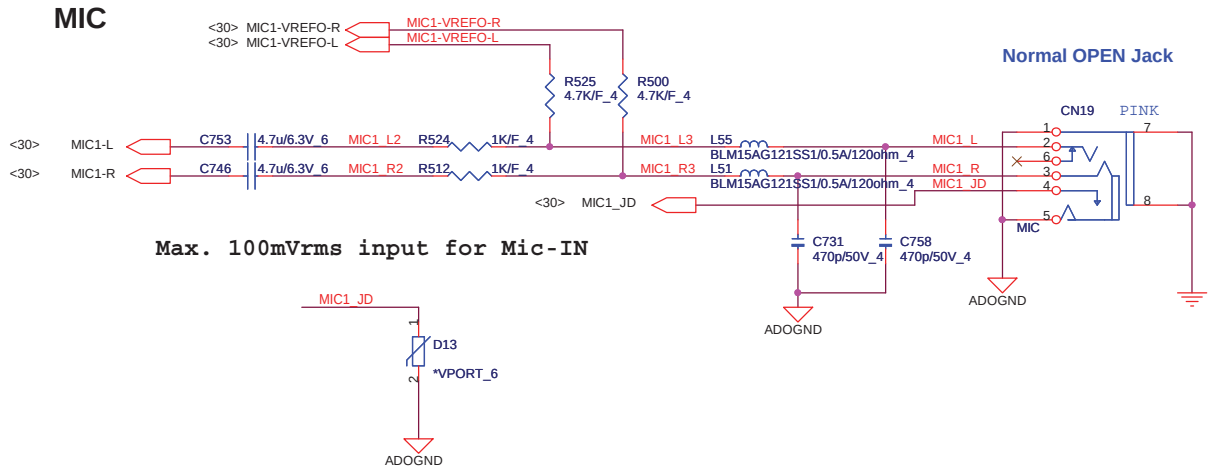
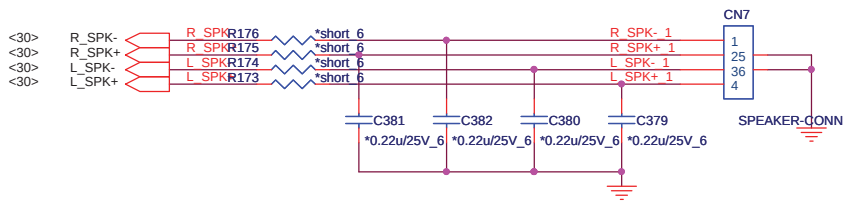
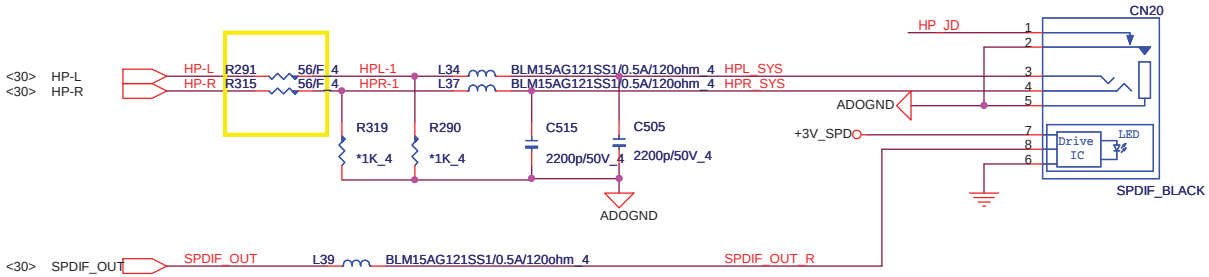
MIC

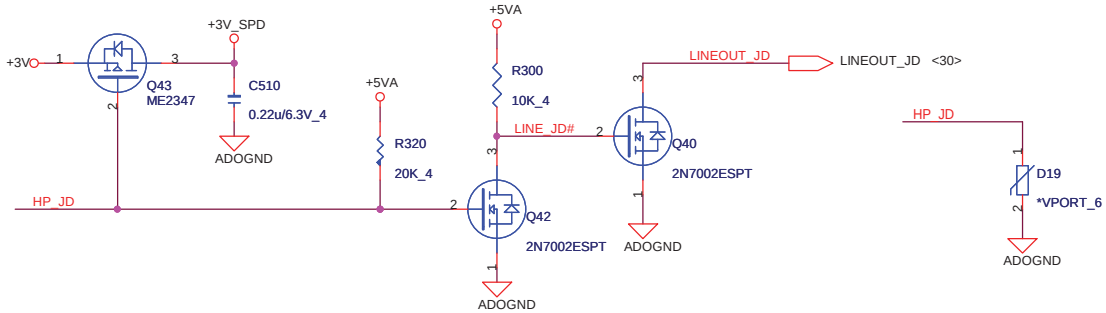


Internal Speaker



HP/SPDIF





Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A

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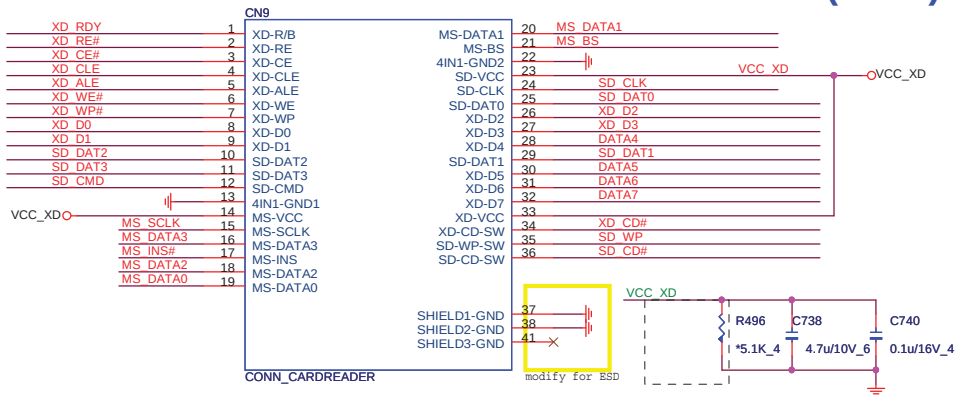
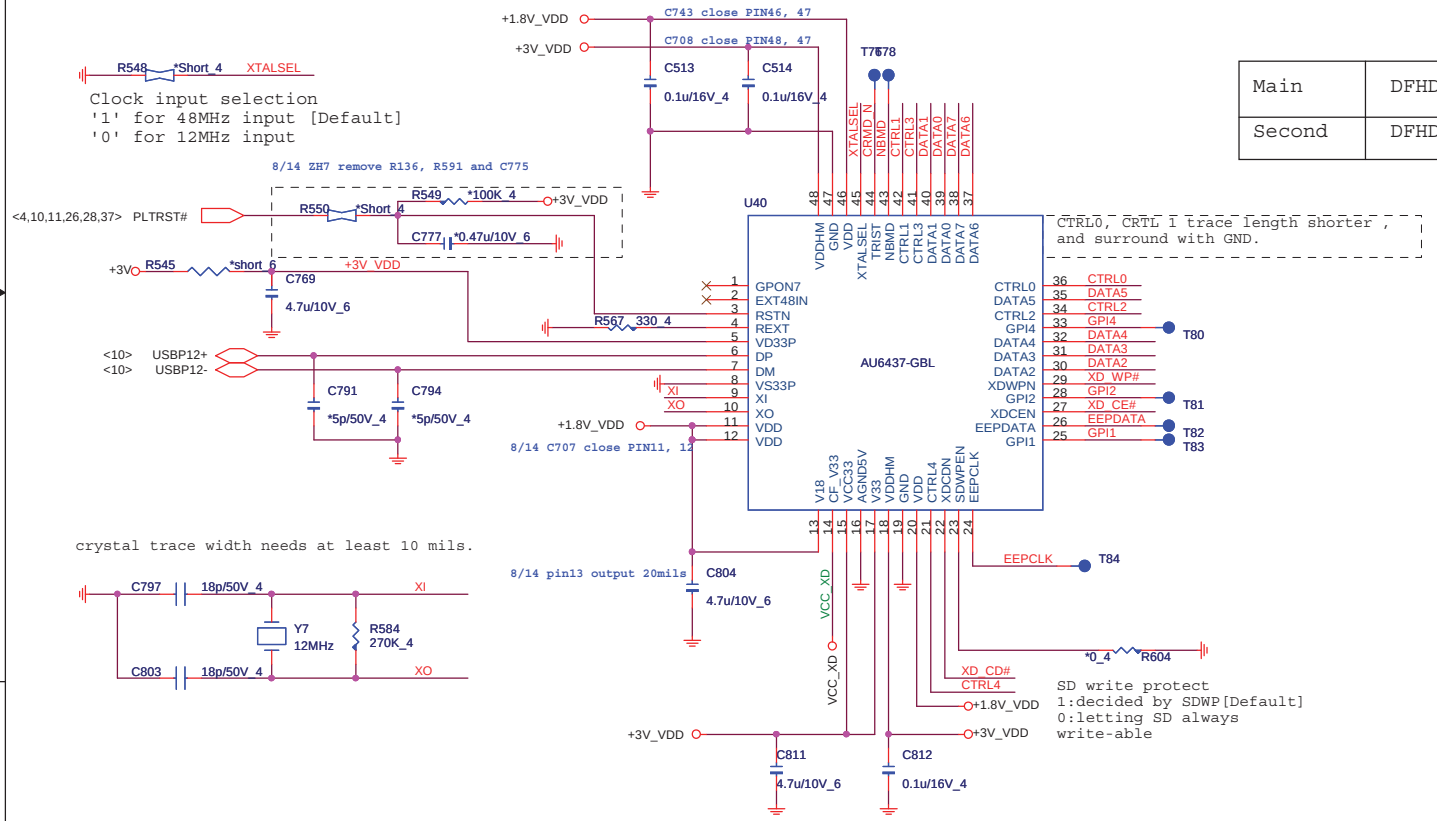
CARD READER Controller

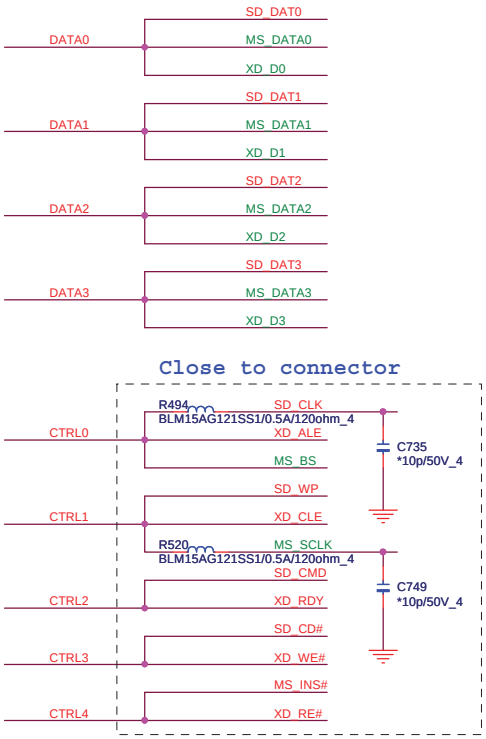
4 IN 1 CARD READER (MMC)



Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

Main	DFHD36MS006
Second	DFHD36MS012





Quanta Computer Inc.

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Size	Document Number	Rev
	AU6433 CardReader	1A

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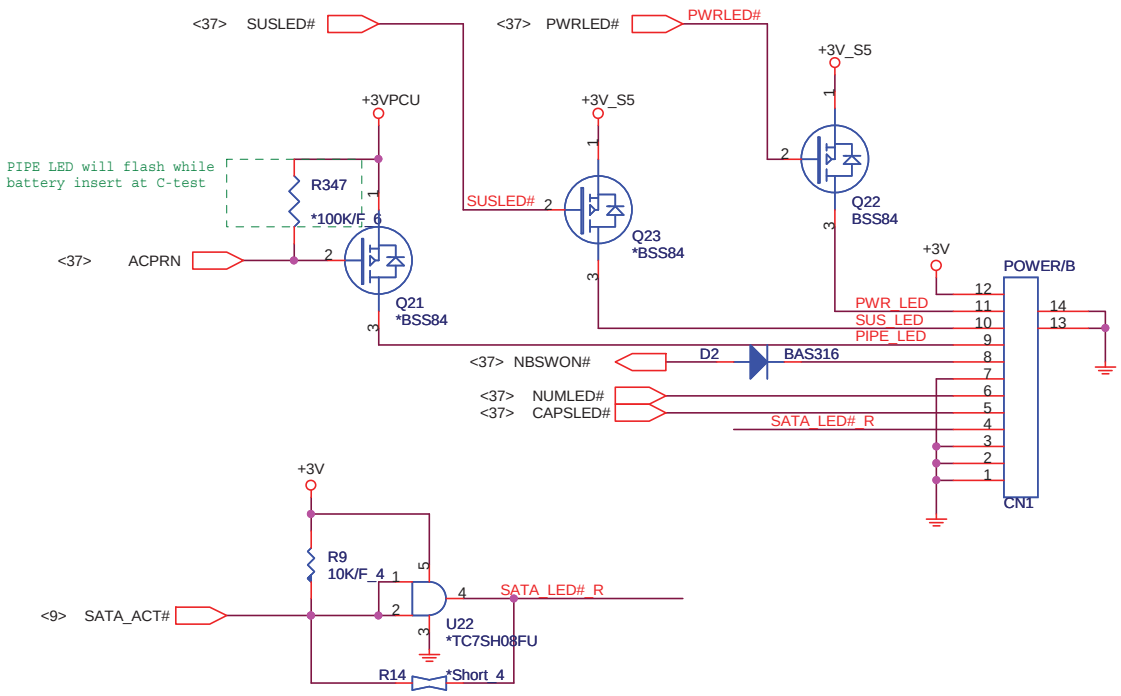
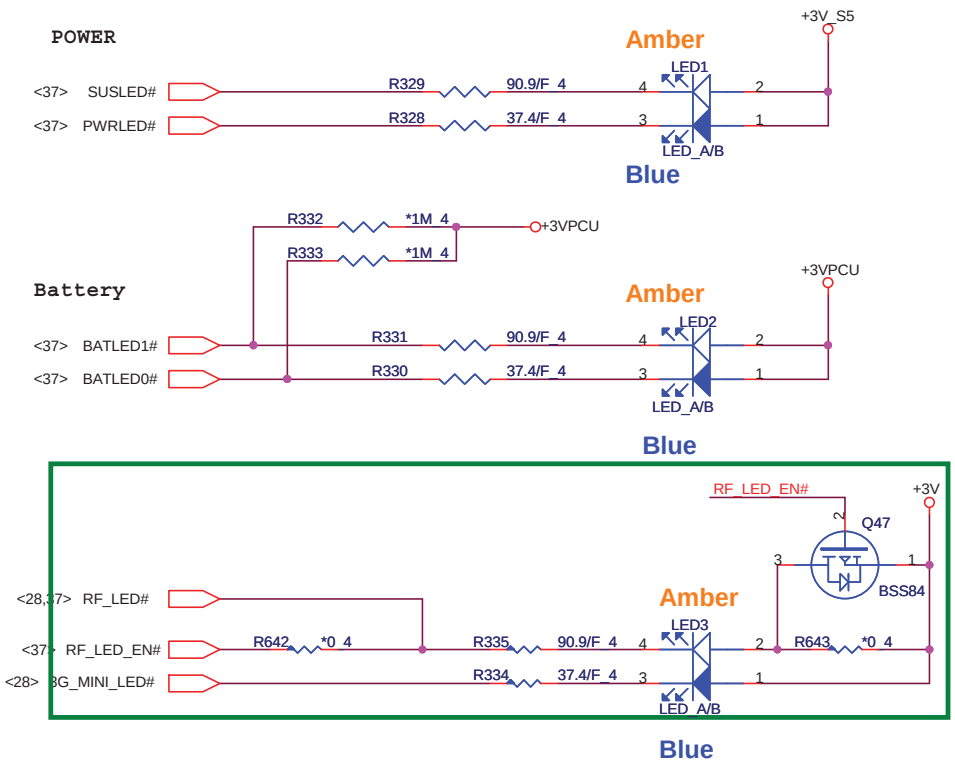
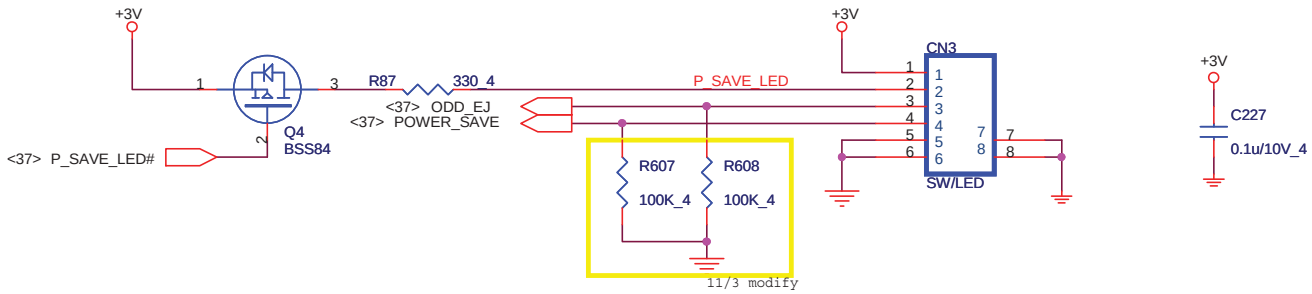
POWER BOARD CONN(UIF)



LED



SW /B



Quanta Computer Inc.

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Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A

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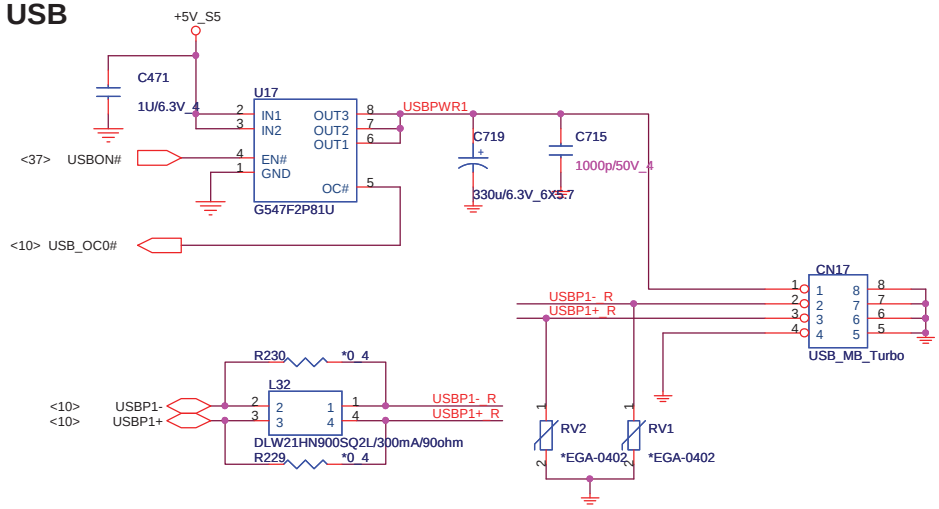
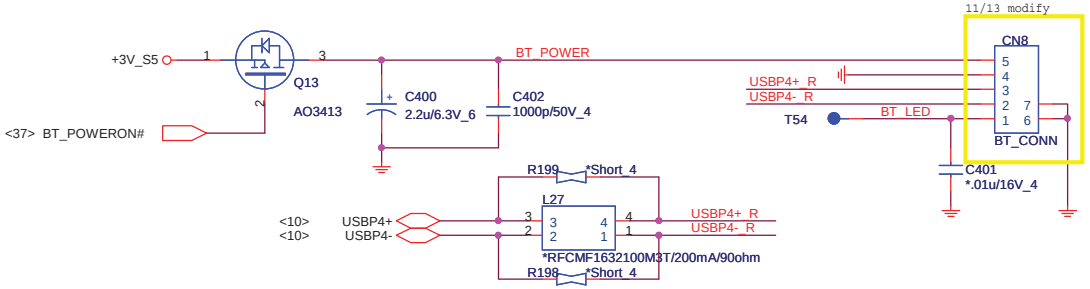
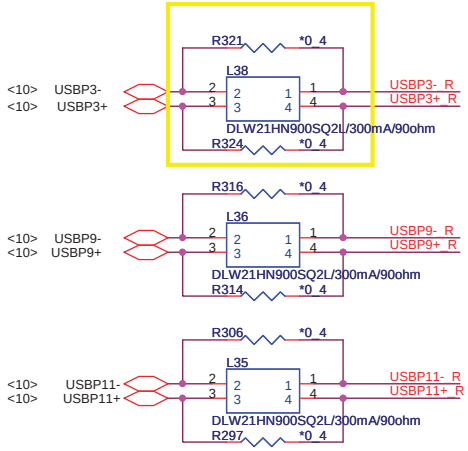
USB

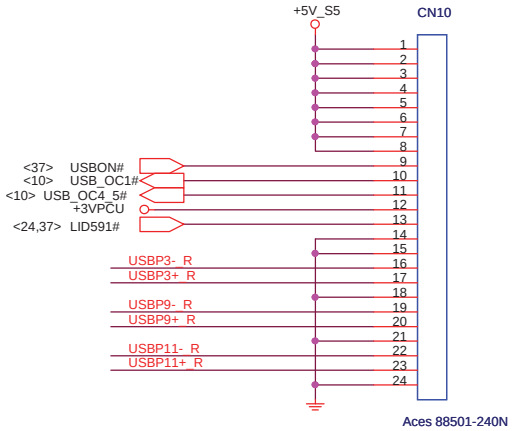


BLUETOOTH CONNECTOR



USB/B





R230, R229, R321, R324, R316, R314, R306, R297

Quanta Computer Inc.		
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Size	Document Number: USB/ BT	Rev 1A
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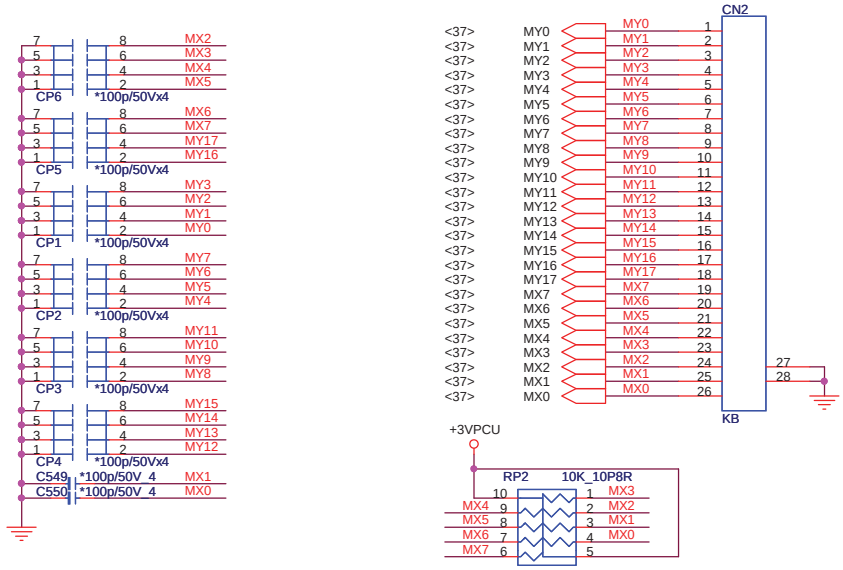
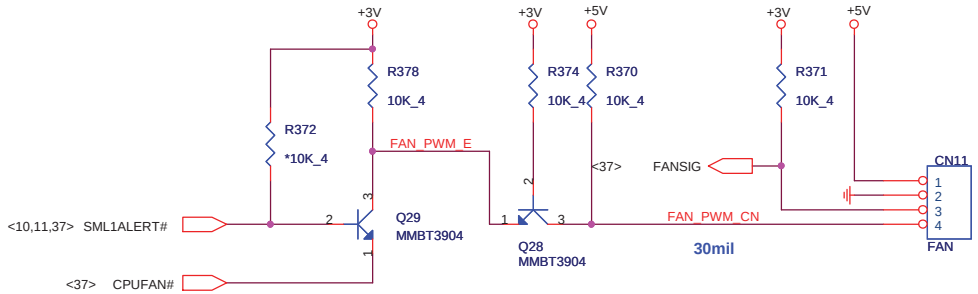
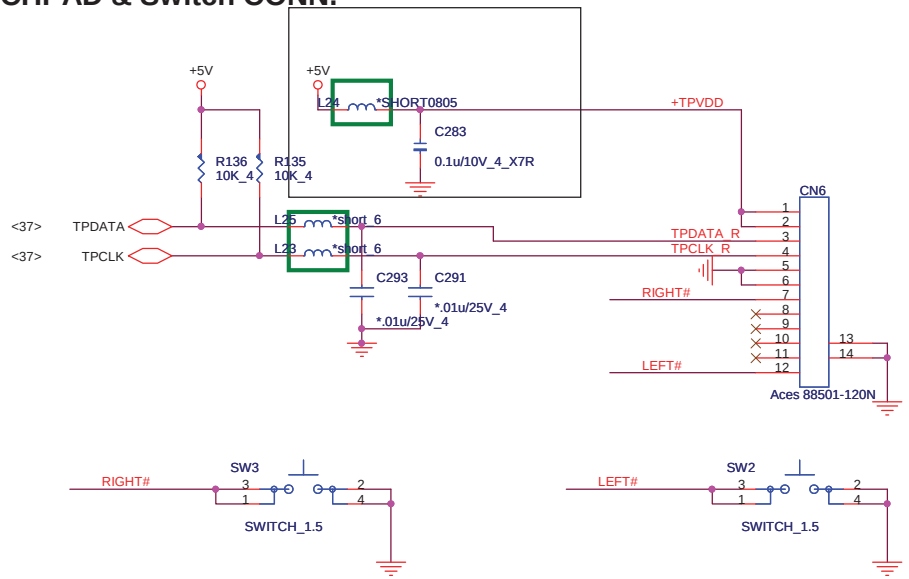
K/B



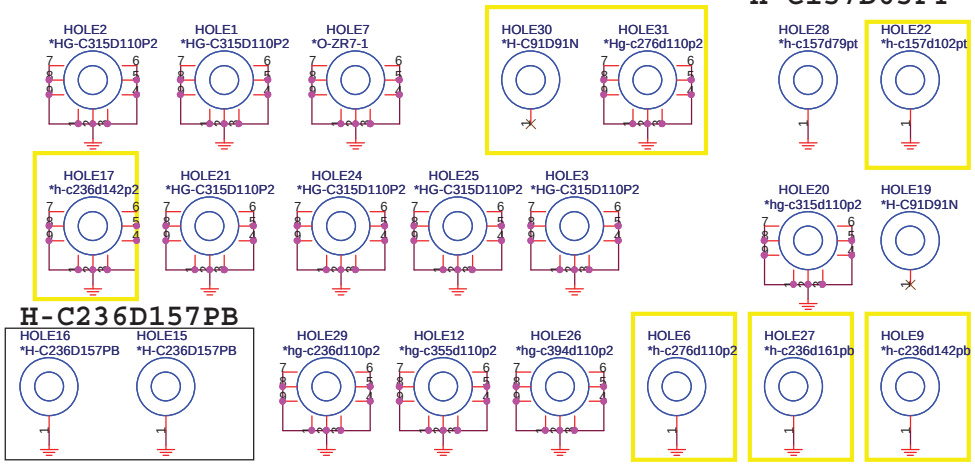
CPU FAN



TOUCHPAD & Switch CONN.

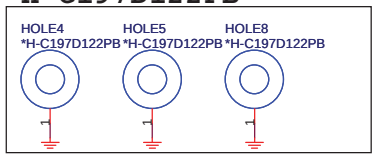


H-C157D63PT

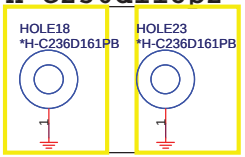


H-C236D157PB

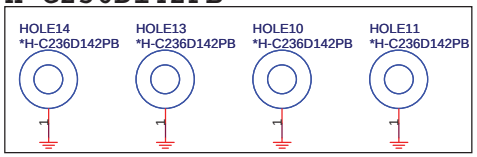
H-C197D122PB



h-c236d118p2



H-C236D142PB



Quanta Computer Inc.

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Size	Document Number	Rev
	KB/FAN/TP+FP	1A

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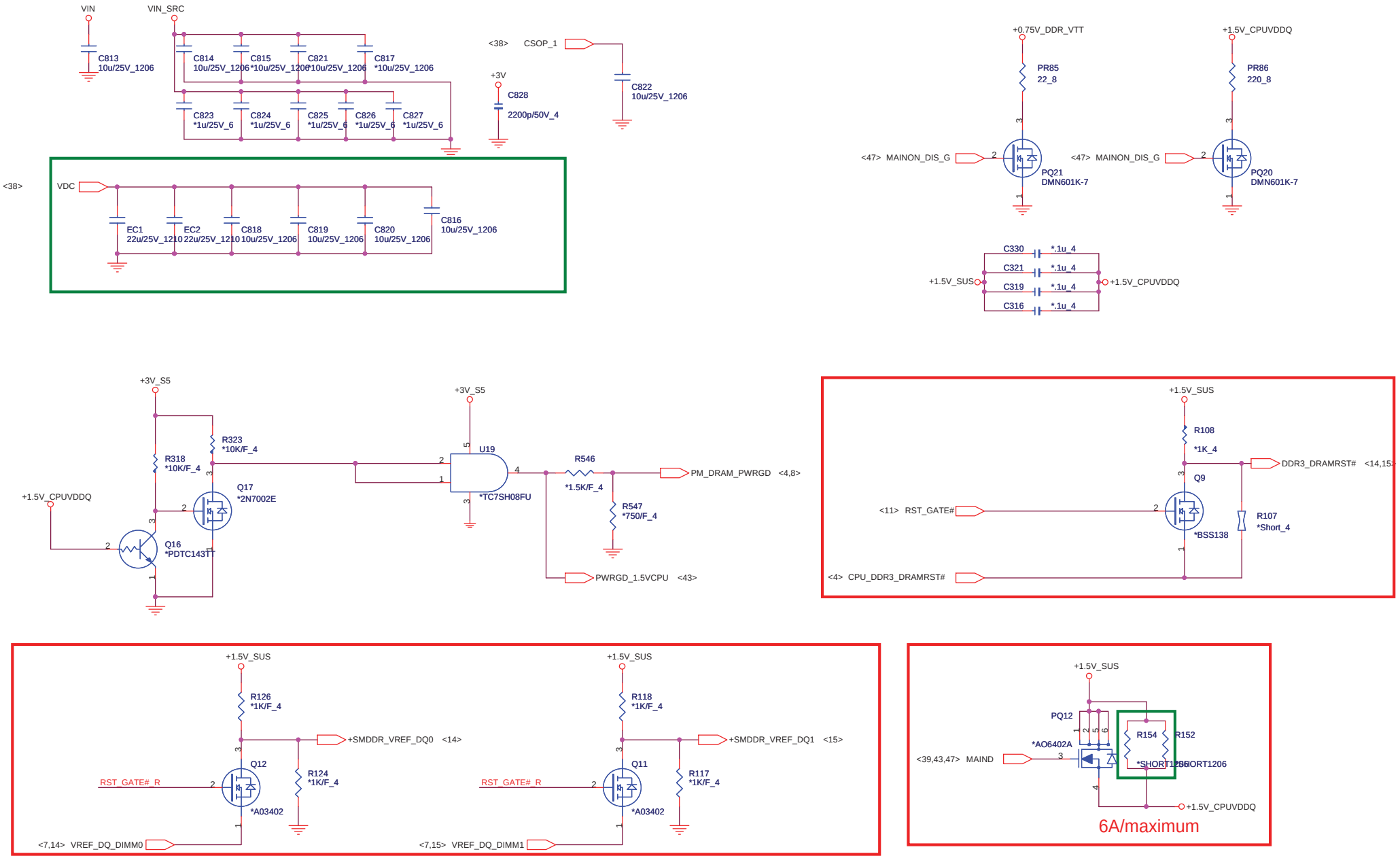
EMI decoupling



Quanta Computer Inc.

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Size	Document Number	Rev
	S3 power saving	1A

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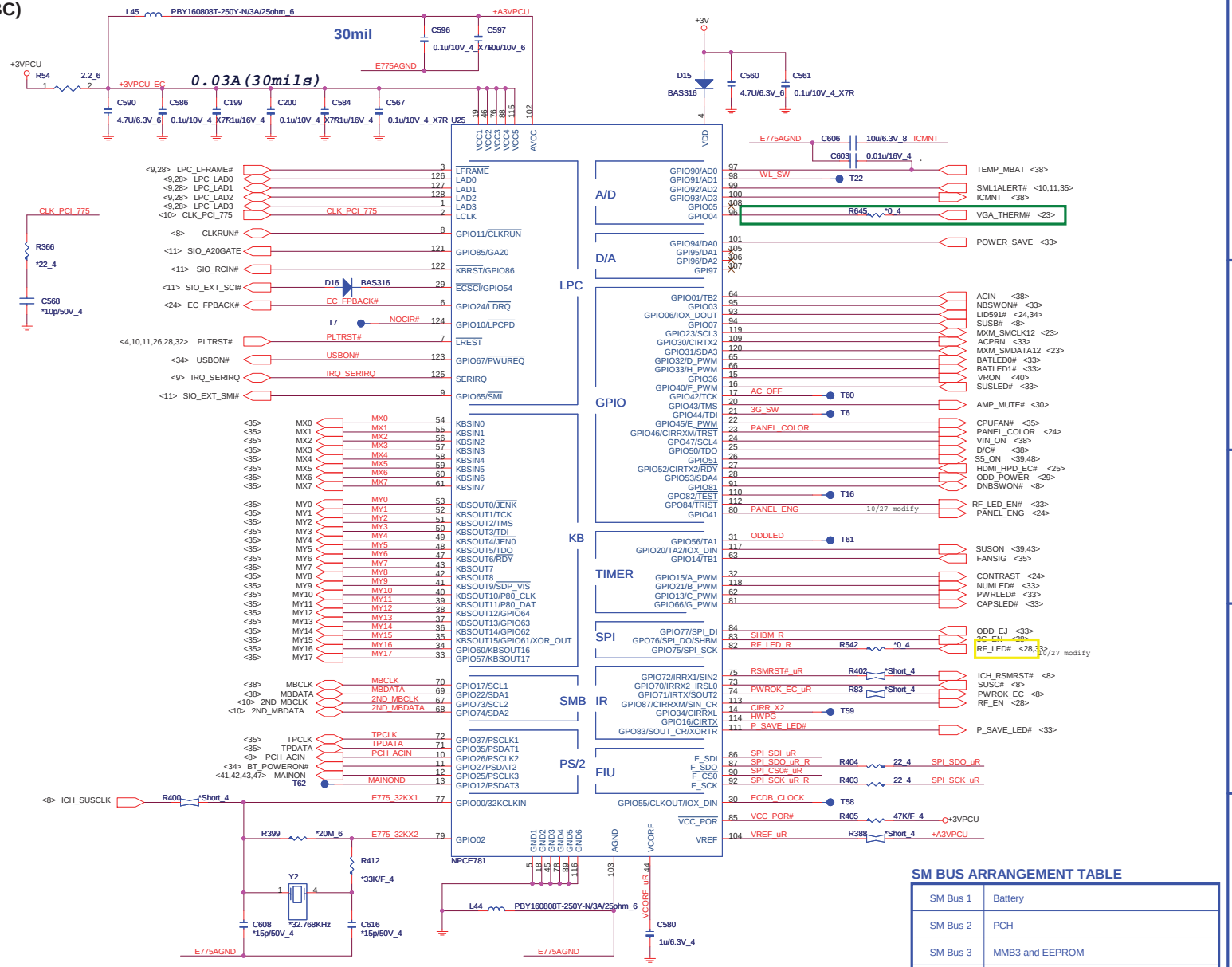
EC(KBC)



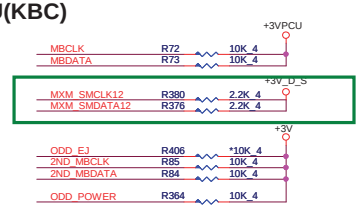
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

SHBM — SHBM_R — R407 — 10K_4

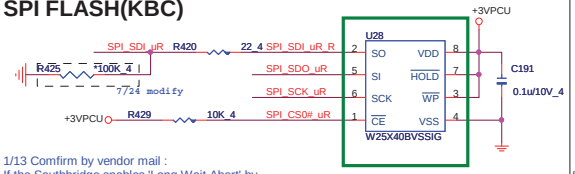
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)



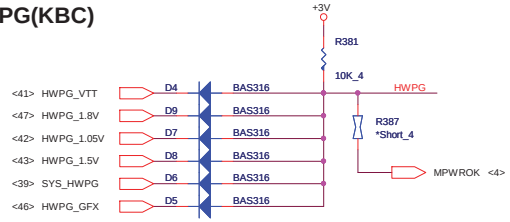
ACER ID(KBC)

SPI FLASH(KBC)

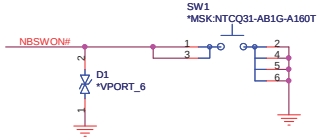


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)



POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.

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	WPCE781 & FLASH	1A

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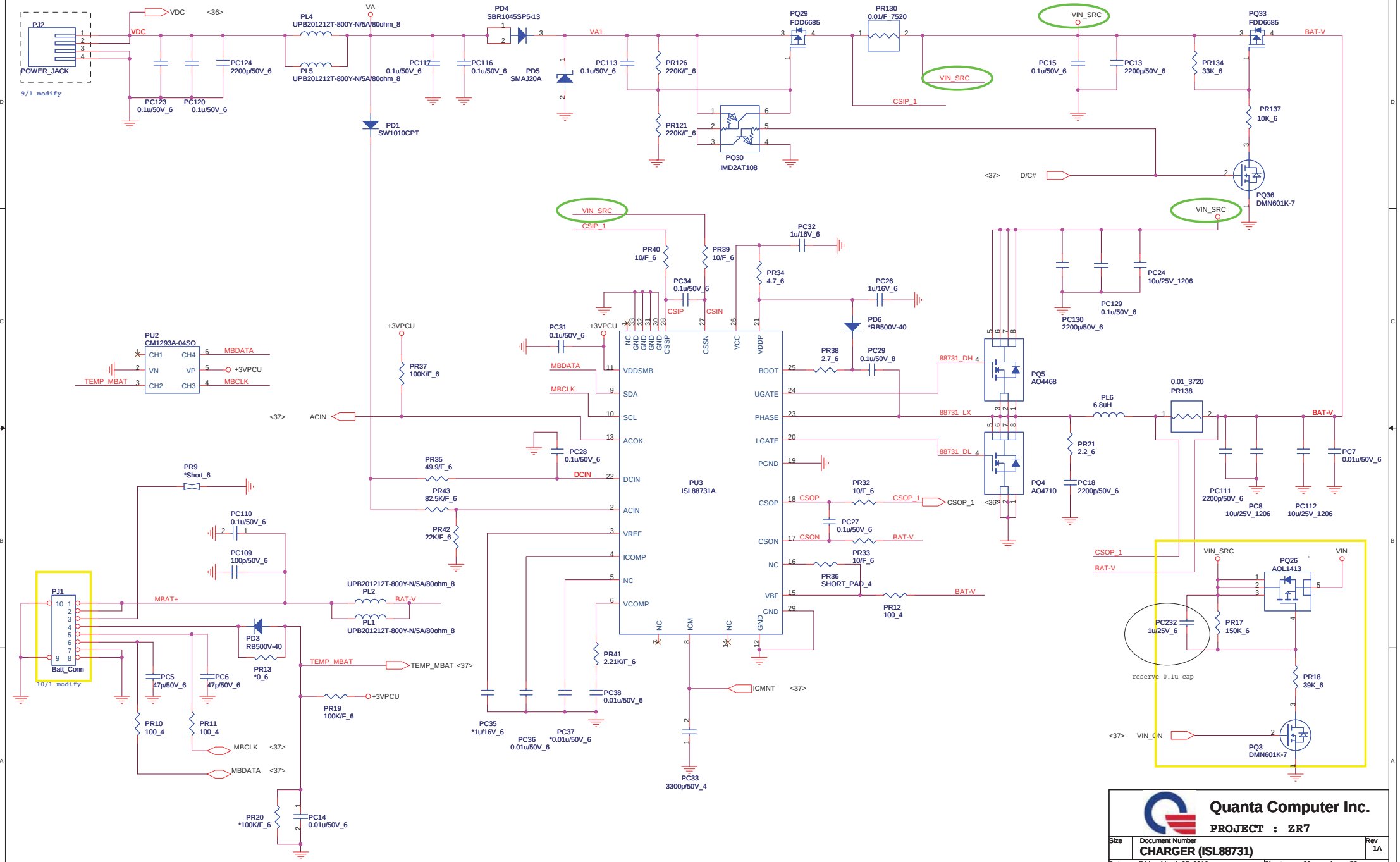

Quanta Computer Inc.

PROJECT : ZR7

Size	Document Number	Rev
	CHARGER (ISL88731)	1A

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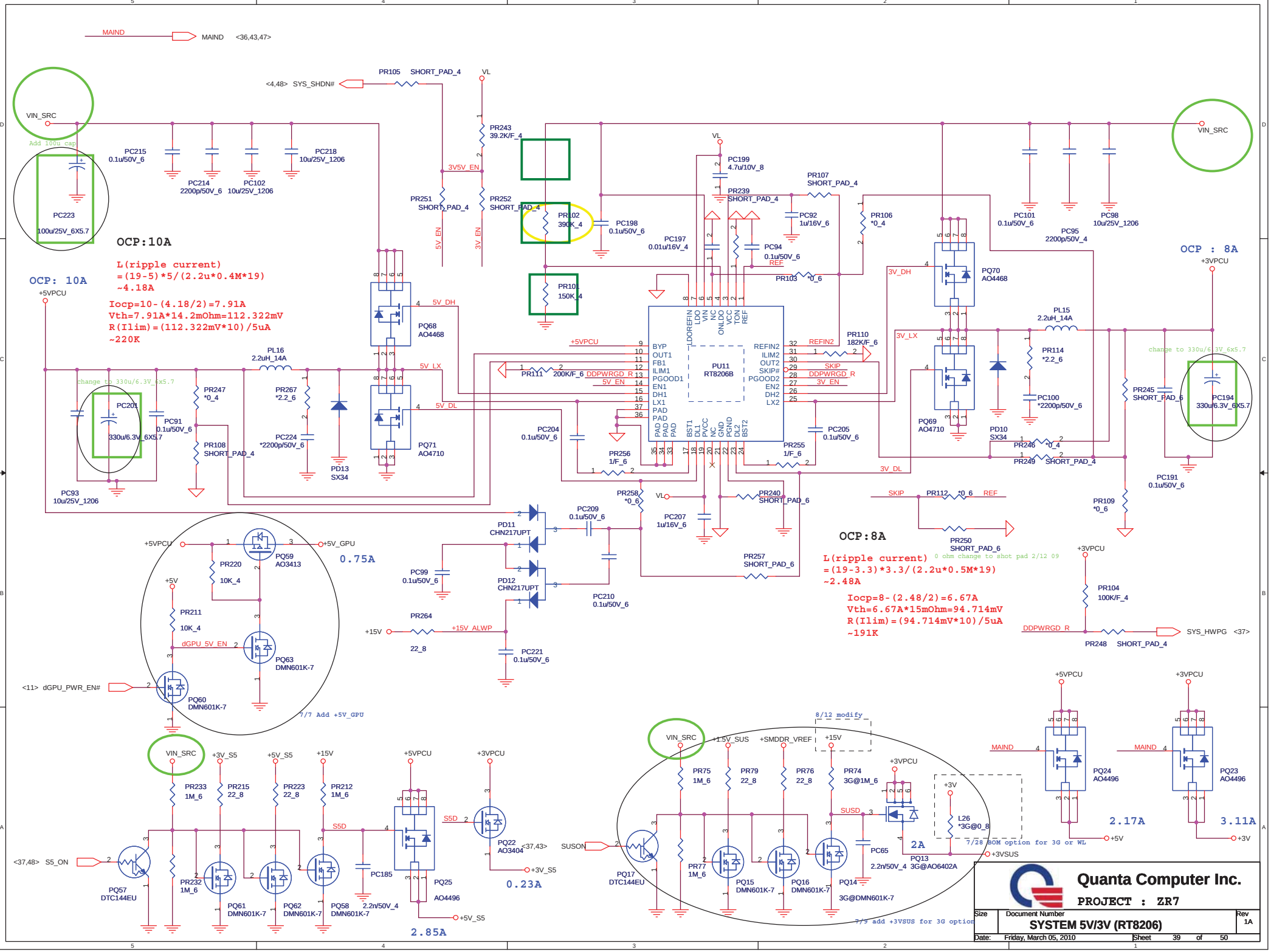
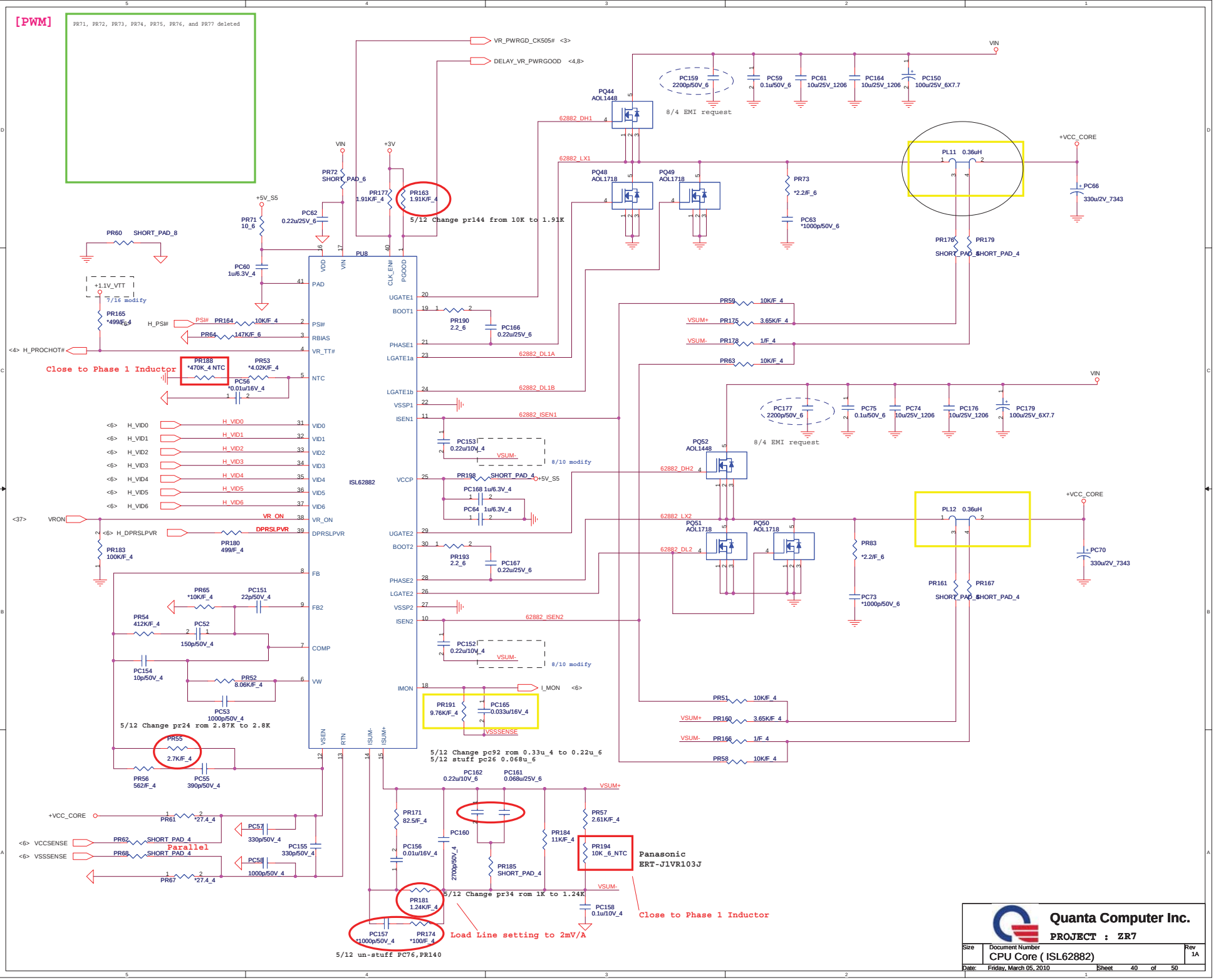
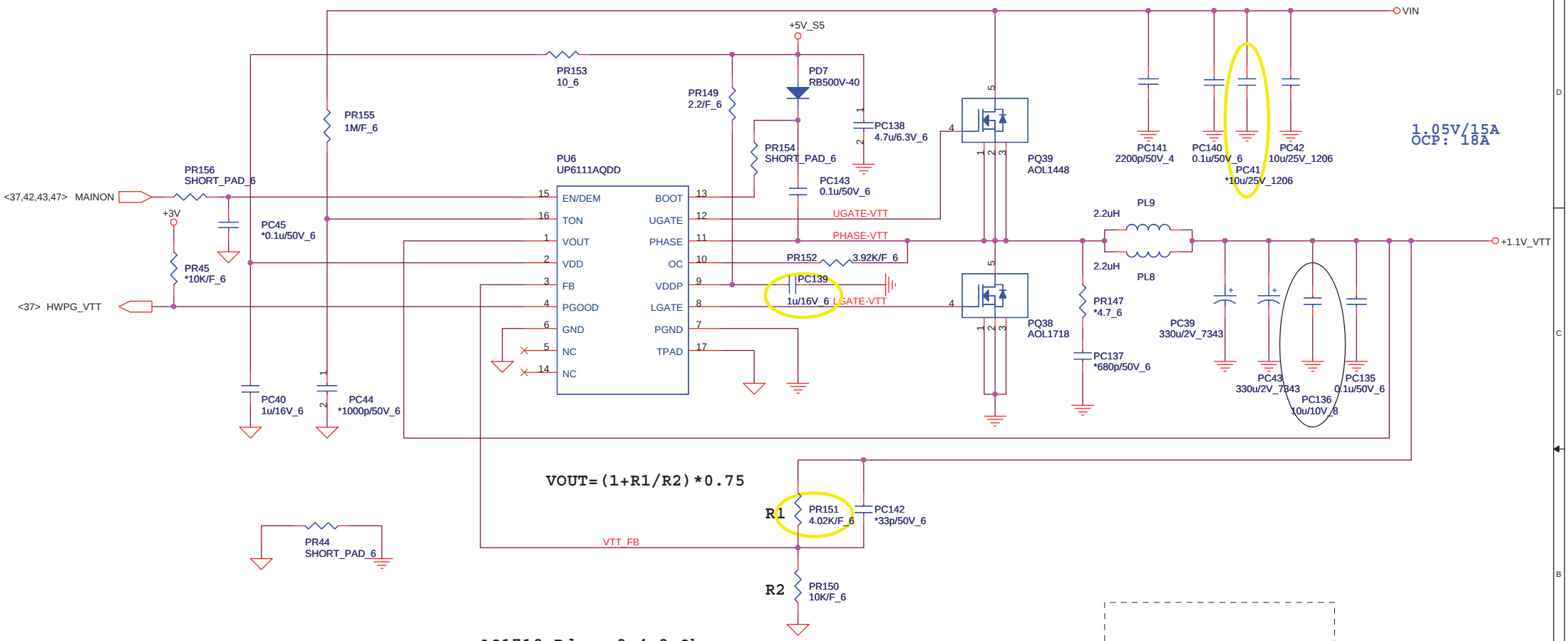

MAIND
MAIND <36,43,47>
<4,48> SYS_SHDN#
PR105 SHORT_PAD_4
VL
VIN_SRC
Add 100u cap
PC223
100u/25V_6X5.7
PC215
0.1u/50V_6
PC214
2200p/50V_6
PC102
10u/25V_1206
PC218
10u/25V_1206
3V5V_EN
PR251
SHORT_PAD_4
PR252
SHORT_PAD_4
5V_EN
3V_EN
PR243
39.2K/F_4
PR102
390K_4
PR101
150K_4
PC198
0.1u/50V_6
PC197
0.01u/16V_4
PC199
4.7u/10V_8
PR239
SHORT_PAD_4
PC92
1u/16V_6
PR107
SHORT_PAD_4
PR106
*0_4
PC94
0.1u/50V_6
REF
PR103
*0_6
PC101
0.1u/50V_6
PC95
2200p/50V_4
PC98
10u/25V_1206
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP: 10A
+5VPCU
PQ68
AO4468
5V_DH
5V_LX
PQ71
AO4710
5V_DL
PL16
2.2uH_14A
change to 330u/6.3V_6x5.7
PC201
330u/6.3V_6X5.7
PC91
0.1u/50V_6
PR247
*0_4
PR108
SHORT_PAD_4
PC93
10u/25V_1206
PR267
*2.2_6
PC224
*2200p/50V_6
PD13
SX34
PR111
200K/F_6
DDPWRGD_R
5V_EN
PU11
RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DL1
PVCC
GND
PGND
DL2
BST2
REFIN2
SKIP
DDPWRGD_R
3V_EN
PR110
182K/F_6
PC204
0.1u/50V_6
PR256
1/F_6
PC205
0.1u/50V_6
PR255
1/F_6
3V_DH
3V_LX
3V_DL
PQ70
AO4468
PQ69
AO4710
PL15
2.2uH_14A
PR114
*2.2_6
PC100
*2200p/50V_6
PD10
SX34
PR246
*0_4
PR249
SHORT_PAD_4
OCP : 8A
+3VPCU
change to 330u/6.3V_6x5.7
PC194
330u/6.3V_6X5.7
PR245
SHORT_PAD_6
PC191
0.1u/50V_6
PR109
*0_6
PR258
*0_6
PR240
SHORT_PAD_6
PC207
1u/16V_6
PR257
SHORT_PAD_6
SKIP
PR112
*0_6
REF
PR250
SHORT_PAD_6
0 ohm change to shot pad 2/12 09
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
PD11
CHN217UPT
PD12
CHN217UPT
PC209
0.1u/50V_6
PC99
0.1u/50V_6
PC210
0.1u/50V_6
PR264
22_8
+15V
+15V_ALWP
PC221
0.1u/50V_6
+3VPCU
PR104
100K/F_4
DDPWRGD_R
PR248
SHORT_PAD_4
SYS_HWPG <37>
+5VPCU
PQ59
AO3413
+5V_GPU
0.75A
PR220
10K_4
+5V
PR211
10K_4
dGPU_5V_EN
PQ63
DMN601K-7
<11> dGPU_PWR_EN#
PQ60
DMN601K-7
7/7 Add +5V_GPU
VIN_SRC
+3V_S5
+5V_S5
+15V
+5VPCU
+3VPCU
PR233
1M_6
PR215
22_8
PR223
22_8
PR212
1M_6
S5D
PQ25
AO4496
PQ22
AO3404
<37,43>
+3V_S5
0.23A
<37,48> S5_ON
PQ57
DTC144EU
PR232
1M_6
PQ61
DMN601K-7
PQ62
DMN601K-7
PQ58
DMN601K-7
PC185
2.2n/50V_4
+5V_S5
2.85A
8/12 modify
VIN_SRC
+1.5V_SUS
+SMDDR_VREF
+15V
PR75
1M_6
PR79
22_8
PR76
22_8
PR74
3G@1M_6
SUSD
SUSON
PQ17
DTC144EU
PR77
1M_6
PQ15
DMN601K-7
PQ16
DMN601K-7
PQ14
3G@DMN601K-7
PC65
2.2n/50V_4
PQ13
3G@AO6402A
2A
+3V
L26
*3G@0_8
7/28 BOM option for 3G or WL
+3VSUS
7/9 add +3VSUS for 3G option
MAIND
PQ24
AO4496
2.17A
+5V
PQ23
AO4496
3.11A
+3V
Quanta Computer Inc.
PROJECT : ZR7
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev
1A
Date: Friday, March 05, 2010
Sheet 39 of 50


[PWM]
PR71, PR72, PR73, PR74, PR75, PR76, and PR77 deleted
VR_PWRGD_CK505# <3>
DELAY_VR_PWRGOOD <4,8>
VIN
+3V
+5V_S5
PR72 SHORT_PAD_6
PR177 1.91K/F_4
PR163 1.91K/F_4
5/12 Change pr144 from 10K to 1.91K
PR71 10_6
PC62 0.22u/25V_6
PR60 SHORT_PAD_8
PC60 1u/6.3V_4
+1.1V_VTT
7/16 modify
PR165 *499/F_4
H_PSI#
PR164 10K/F_4
PR64 147K/F_6
<4> H_PROCHOT#
Close to Phase 1 Inductor
PR188 *470K_4 NTC
PR53 *4.02K/F_4
PC56 *0.01u/16V_4
PU8
ISL62882
VDD
VIN
CLK_EN#
PGOOD
PAD
PSI#
RBIAS
VR_TT#
NTC
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
FB
FB2
COMP
VW
VSEN
RTN
ISUM-
ISUM+
UGATE1
BOOT1
PHASE1
LGATE1a
LGATE1b
VSSP1
ISEN1
VCCP
UGATE2
BOOT2
PHASE2
LGATE2
VSSP2
ISEN2
IMON
<6> H_VID0
<6> H_VID1
<6> H_VID2
<6> H_VID3
<6> H_VID4
<6> H_VID5
<6> H_VID6
<37> VRON
<6> H_DPRSLPVR
PR183 100K/F_4
PR180 499/F_4
PR65 *10K/F_4
PC151 22p/50V_4
PR54 412K/F_4
PC52 150p/50V_4
PC154 10p/50V_4
PR52 8.06K/F_4
PC53 1000p/50V_4
5/12 Change pr24 rom 2.87K to 2.8K
PR55 2.7K/F_4
PR56 562/F_4
PC55 390p/50V_4
+VCC_CORE
PR61 *27.4_4
PC57 330p/50V_4
<6> VCCSENSE
PR62 SHORT_PAD_4
Parallel
<6> VSSSENSE
PR68 SHORT_PAD_4
PC58 1000p/50V_4
PC155 330p/50V_4
PR67 *27.4_4
PR190 2.2_6
PC166 0.22u/25V_6
62882_DH1
62882_LX1
62882_DL1A
62882_DL1B
62882_ISEN1
PC153 0.22u/10V_4
VSUM-
8/10 modify
PR198 SHORT_PAD_4
+5V_S5
PC168 1u/6.3V_4
PC64 1u/6.3V_4
PR193 2.2_6
PC167 0.22u/25V_6
62882_ISEN2
PC152 0.22u/10V_4
I_MON <6>
PR191 9.76K/F_4
PC165 0.033u/16V_4
VSSSENSE
5/12 Change pc92 rom 0.33u_4 to 0.22u_6
5/12 stuff pc26 0.068u_6
PC162 0.22u/10V_6
PC161 0.068u/25V_6
VSUM+
PR171 82.5/F_4
PC160
PC156 0.01u/16V_4
2700p/50V_4
PR185 SHORT_PAD_4
PR184 11K/F_4
PR57 2.61K/F_4
PR194 10K_6_NTC
Panasonic
ERT-J1VR103J
5/12 Change pr34 rom 1K to 1.24K
PR181 1.24K/F_4
PC158 0.1u/10V_4
Close to Phase 1 Inductor
PC157 *1000p/50V_4
PR174 *100/F_4
Load Line setting to 2mV/A
5/12 un-stuff PC76,PR140
PC159 2200p/50V_6
8/4 EMI request
PC59 0.1u/50V_6
PC61 10u/25V_1206
PC164 10u/25V_1206
PC150 100u/25V_6X7.7
PQ44 AOL1448
PQ48 AOL1718
PQ49 AOL1718
PR73 *2.2/F_6
PC63 *1000p/50V_6
PL11 0.36uH
+VCC_CORE
PC66 330u/2V_7343
PR176 SHORT_PAD_4
PR179 SHORT_PAD_4
PR59 10K/F_4
PR175 3.65K/F_4
PR178 1/F_4
PR63 10K/F_4
PC177 2200p/50V_6
PC75 0.1u/50V_6
PC74 10u/25V_1206
PC176 10u/25V_1206
PC179 100u/25V_6X7.7
PQ52 AOL1448
PQ51 AOL1718
PQ50 AOL1718
62882_DH2
62882_LX2
62882_DL2
PR83 *2.2/F_6
PC73 *1000p/50V_6
PL12 0.36uH
PC70 330u/2V_7343
PR161 SHORT_PAD_4
PR167 SHORT_PAD_4
PR51 10K/F_4
PR160 3.65K/F_4
PR166 1/F_4
PR58 10K/F_4
Quanta Computer Inc.
PROJECT : ZR7
Size
Document Number
CPU Core (ISL62882)
Rev 1A
Date: Friday, March 05, 2010
Sheet 40 of 50

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)

=(19-1.05)*1.05/(1u*272k*19)

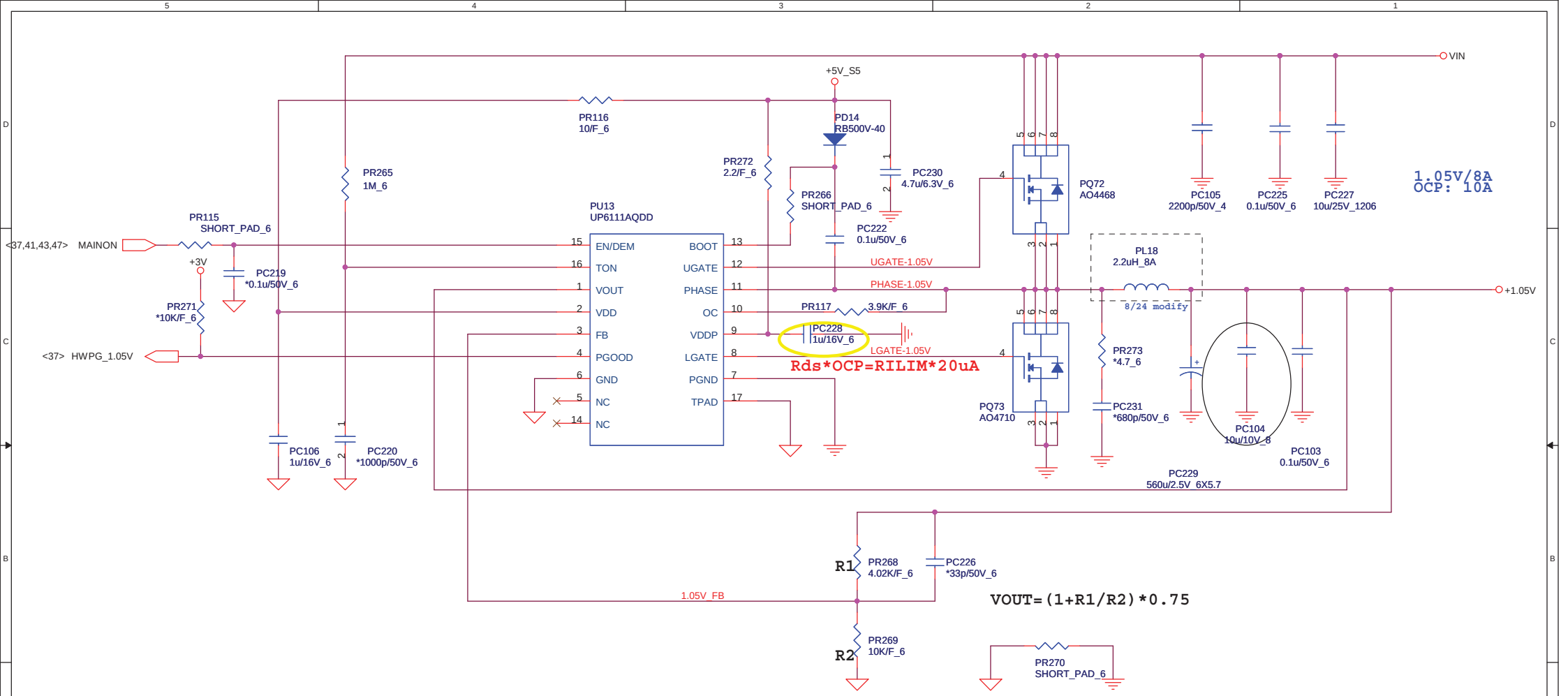
~3.64A

4.3m*18=RILIM*20uA

RILIM=3.87K --- 3.92K

9/4 modify

Quanta Computer Inc.		
PROJECT : ZR7		
Size	Document Number: +VTT (UP6111A)	Rev 1A
Date: Friday, March 05, 2010	Sheet 41 of 50	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA

RILIM=7.1K--- 7.15K

Quanta Computer Inc.

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Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	1A

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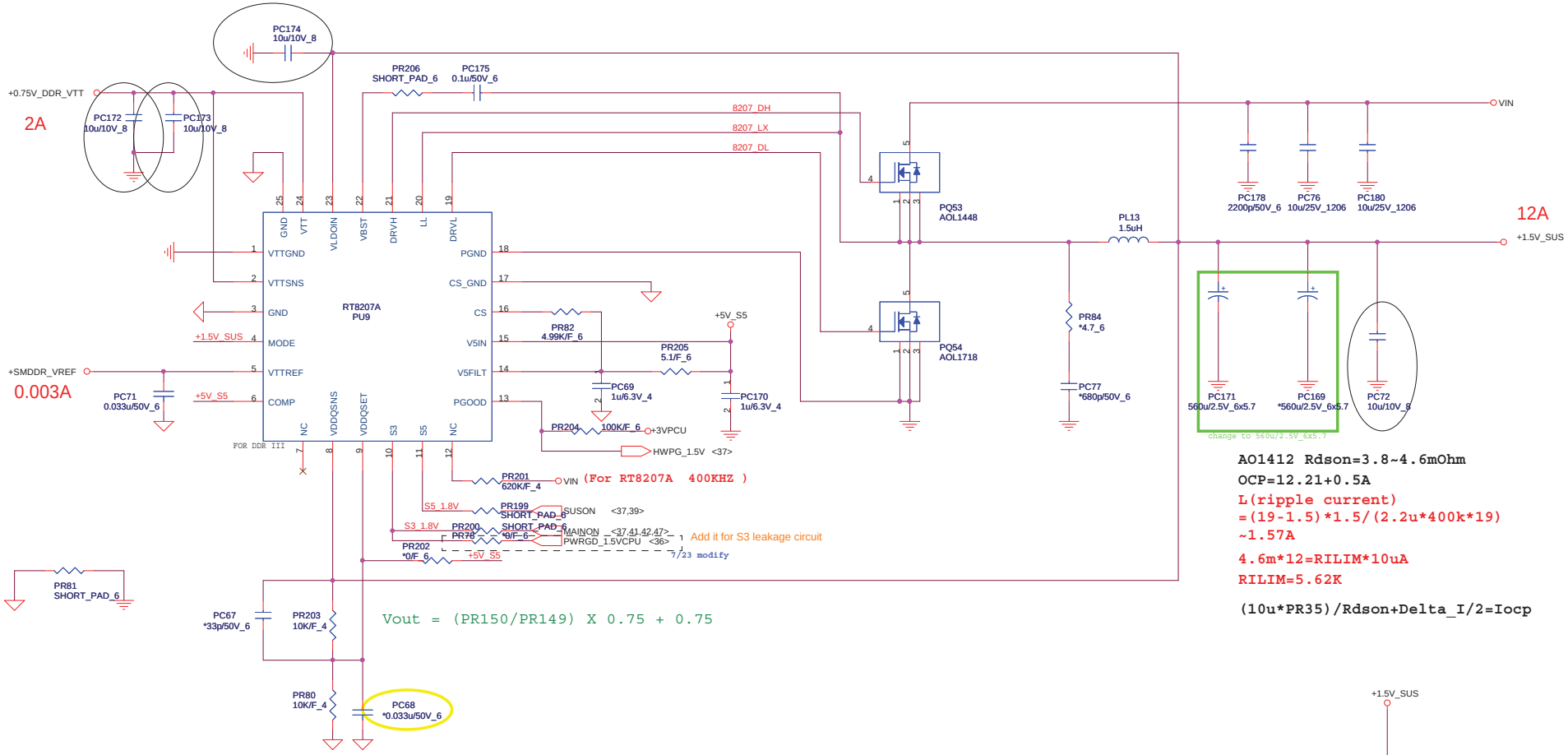

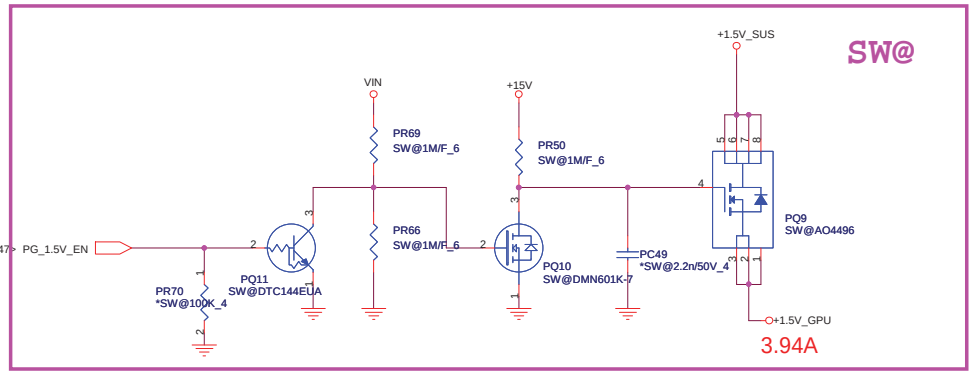

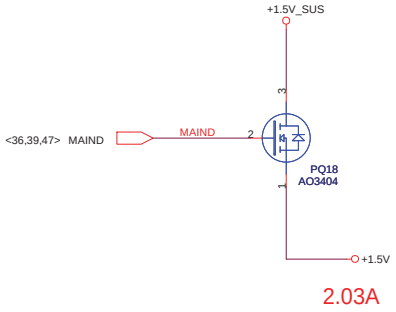

Quanta Computer Inc.

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Size	Document Number	Rev
	DDR III 1.5V(TPS51116)	1A

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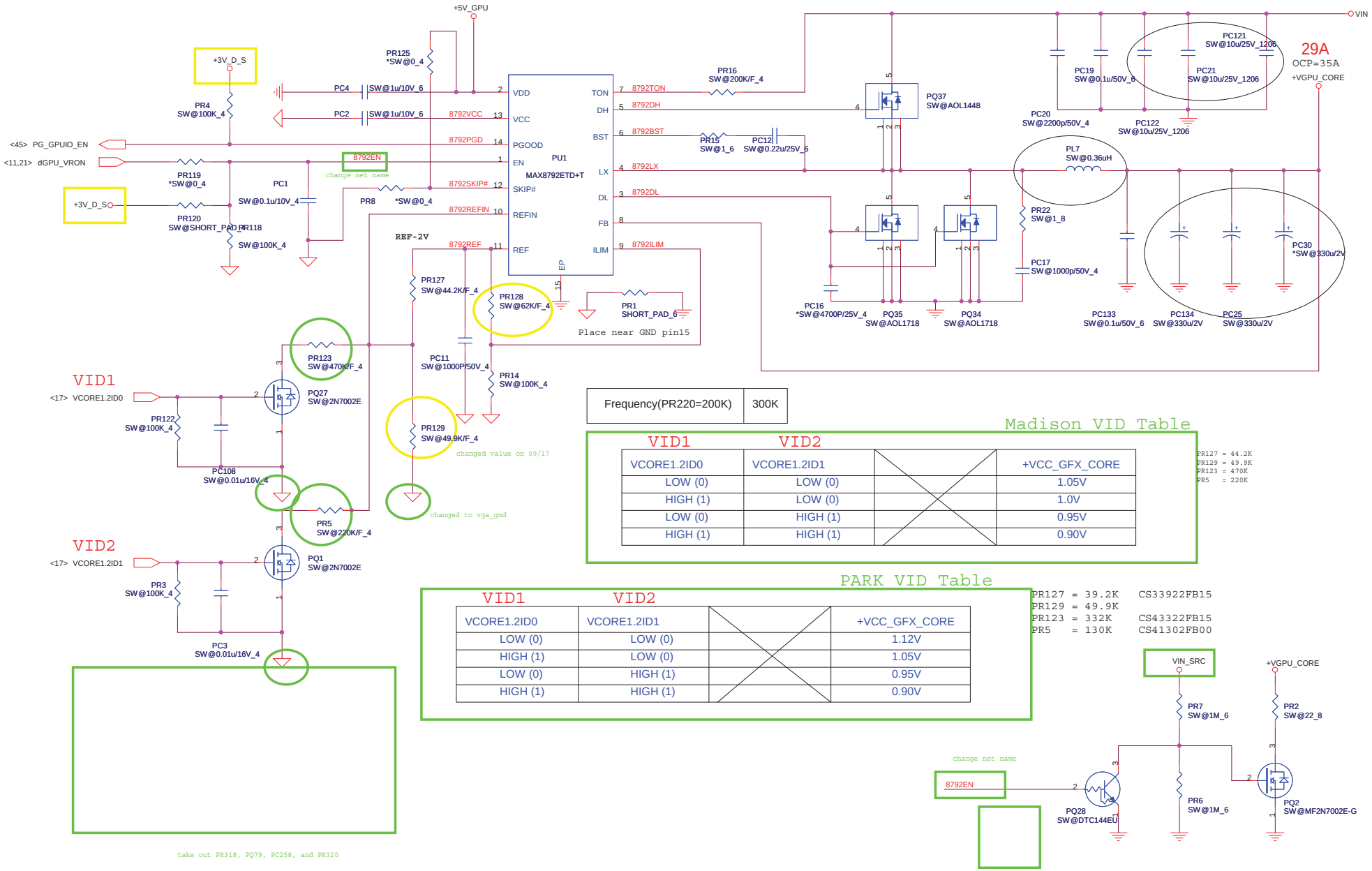

Frequency(PR220=200K)	300K

Madison VID Table

VID1	VID2		
VCORE1.2ID0	VCORE1.2ID1		+VCC_GFX_CORE
LOW (0)	LOW (0)		1.05V
HIGH (1)	LOW (0)		1.0V
LOW (0)	HIGH (1)		0.95V
HIGH (1)	HIGH (1)		0.90V

PR127 = 44.2K
PR129 = 49.9K
PR123 = 470K
PR5 = 220K

PARK VID Table

VID1	VID2		
VCORE1.2ID0	VCORE1.2ID1		+VCC_GFX_CORE
LOW (0)	LOW (0)		1.12V
HIGH (1)	LOW (0)		1.05V
LOW (0)	HIGH (1)		0.95V
HIGH (1)	HIGH (1)		0.90V

PR127 = 39.2K CS33922FB15
PR129 = 49.9K
PR123 = 332K CS43322FB15
PR5 = 130K CS41302FB00

Quanta Computer Inc.

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Size	Document Number	Rev
	GPU CORE(MAX8792)	1A

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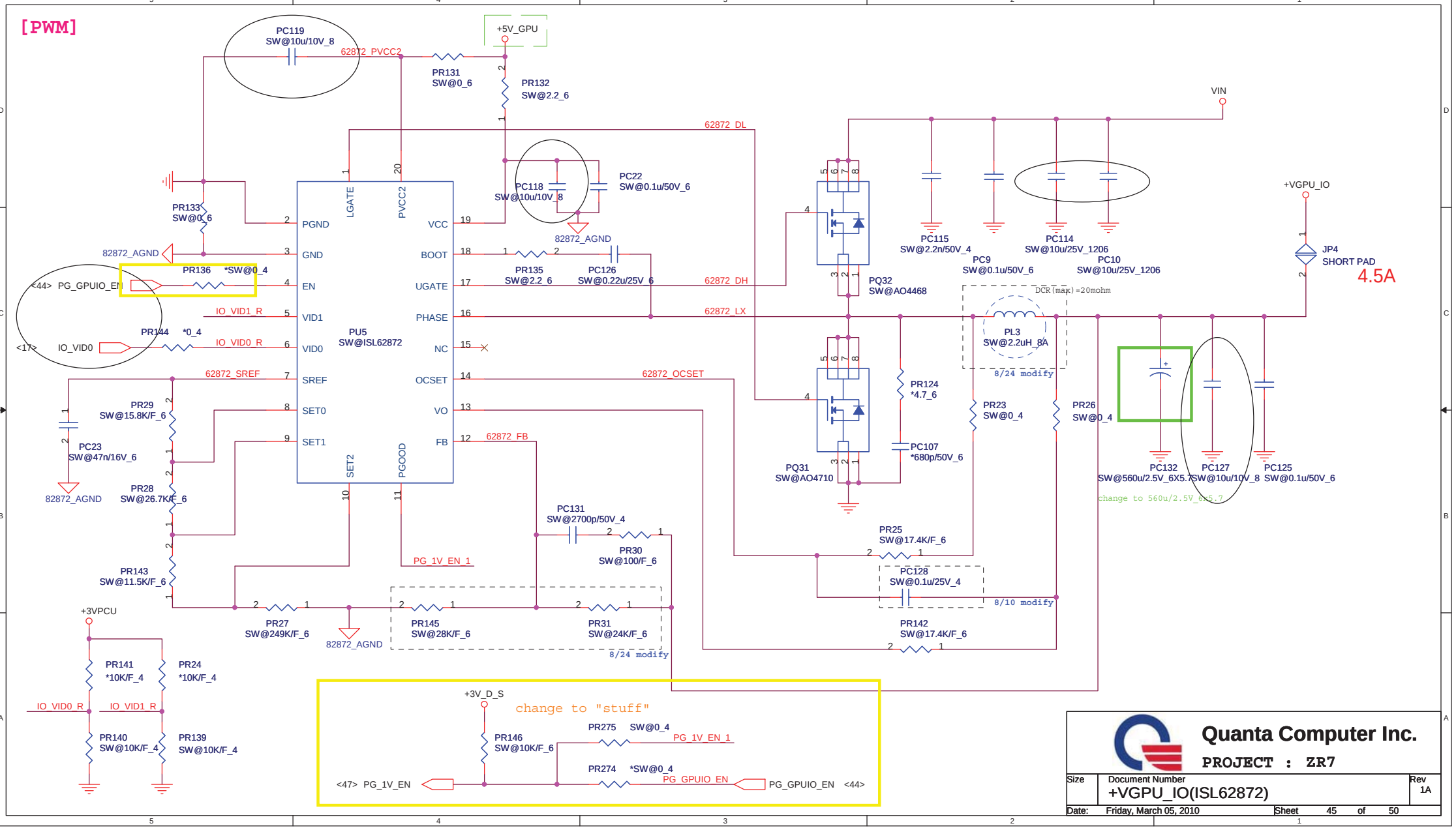

Quanta Computer Inc.

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Size	Document Number	Rev
	+VGPU_IO(ISL62872)	1A

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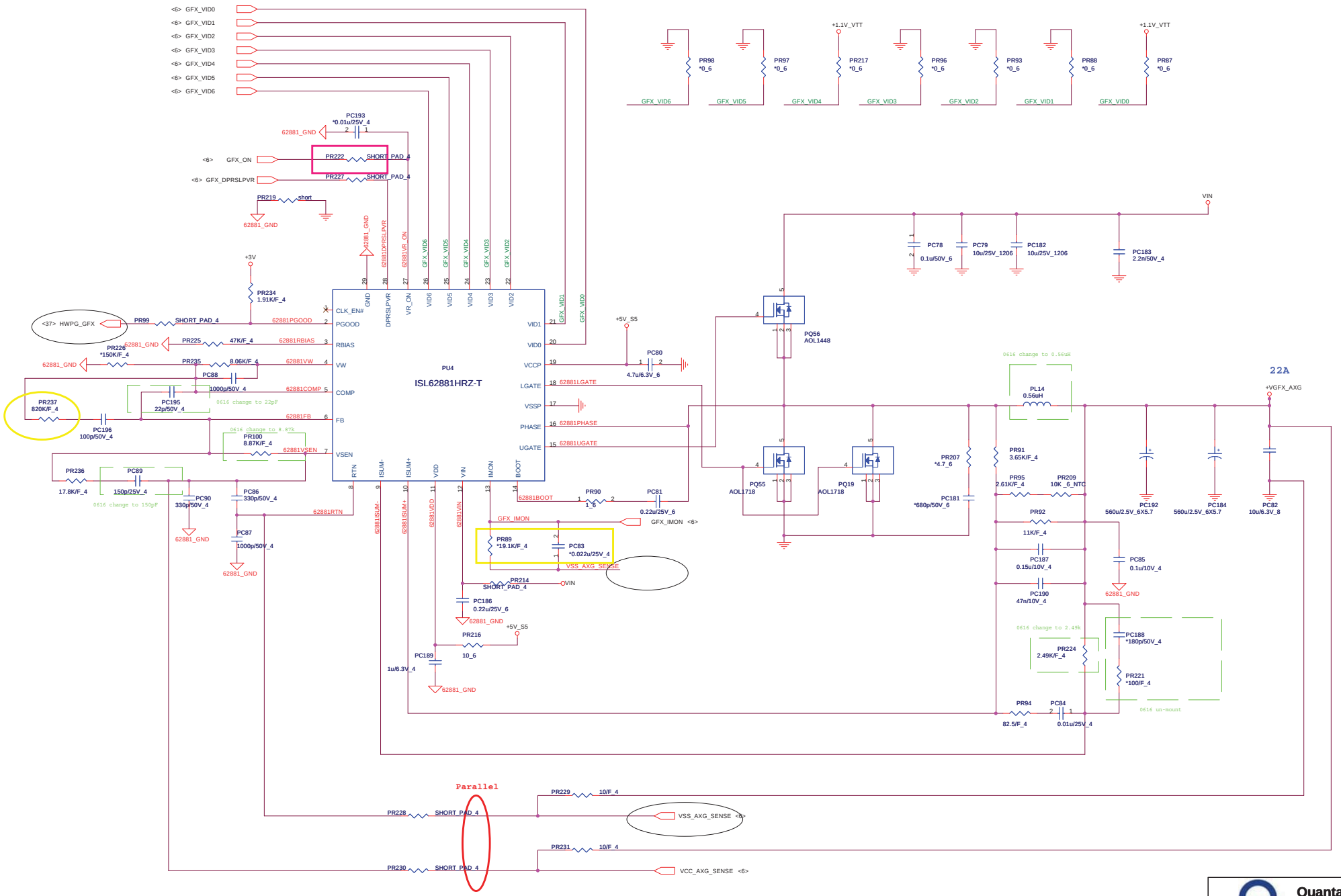
Int_VGA [PWM]



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.

PROJECT : ZR7

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	1A

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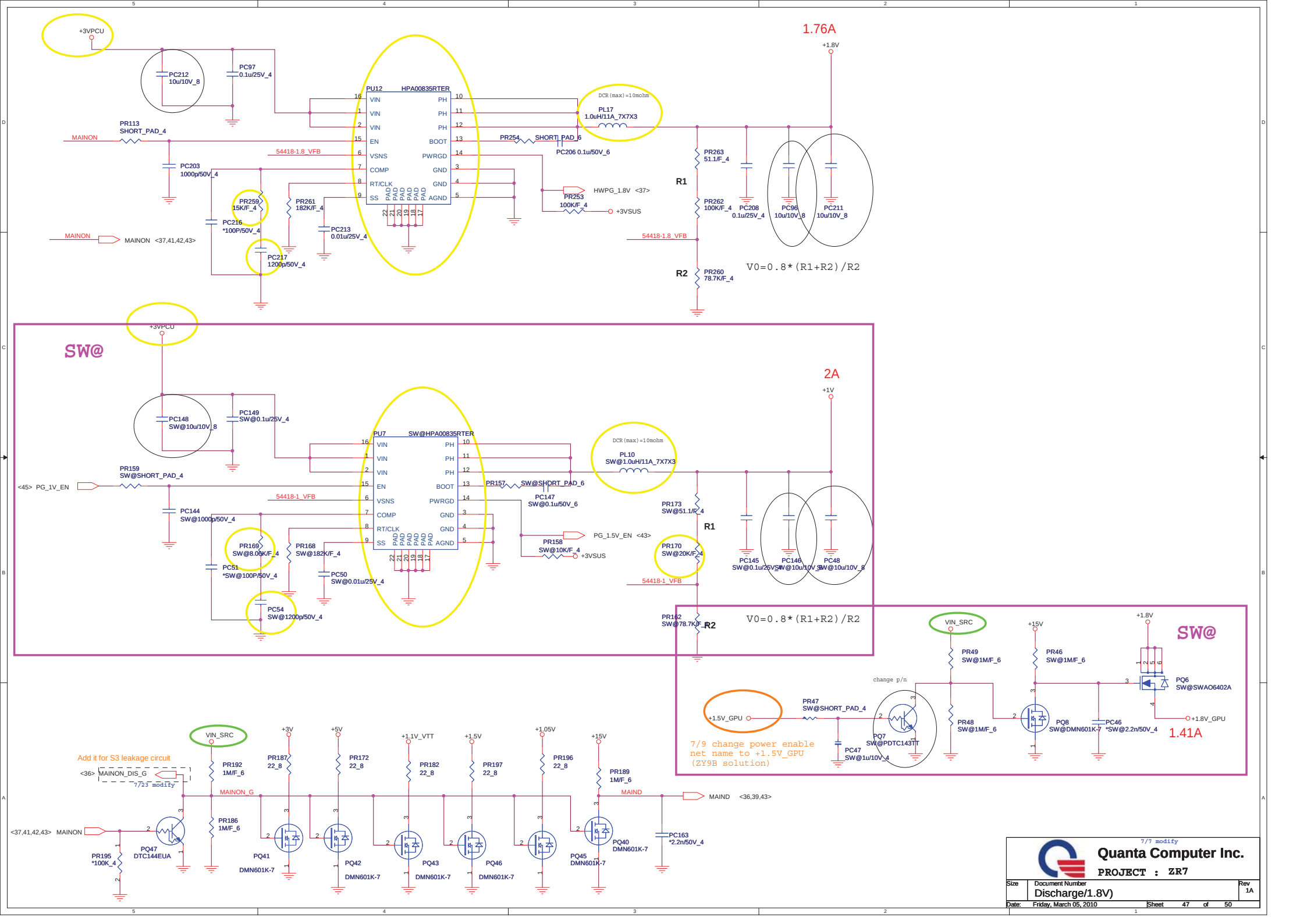
1.76A
+3VPCU
PC212 10u/10V_8
PC97 0.1u/25V_4
PU12 HPA00835RTER
VIN
EN
VSNS
COMP
RT/CLK
SS
PH
BOOT
PWRGD
GND
AGND
PAD
PR113 SHORT_PAD_4
MAINON
PC203 1000p/50V_4
54418-1.8_VFB
PR259 15K/F_4
PR261 182K/F_4
PC216 *100P/50V_4
PC213 0.01u/25V_4
PC217 1200p/50V_4
MAINON <37,41,42,43>
DCR(max)=10mohm
PL17 1.0uH/11A_7X7X3
PR254 SHORT_PAD_6
PC206 0.1u/50V_6
PR253 100K/F_4
HWPG_1.8V <37>
+3VSUS
+1.8V
R1
R2
PR263 51.1/F_4
PR262 100K/F_4
PR260 78.7K/F_4
PC208 0.1u/25V_4
PC96 10u/10V_8
PC211 10u/10V_8
V0=0.8*(R1+R2)/R2
SW@
2A
+1V
PC148 SW@10u/10V_8
PC149 SW@0.1u/25V_4
PU7 SW@HPA00835RTER
PR159 SW@SHORT_PAD_4
<45> PG_1V_EN
PC144 SW@1000p/50V_4
54418-1_VFB
PR169 SW@8.06K/F_4
PR168 SW@182K/F_4
PC51 *SW@100P/50V_4
PC50 SW@0.01u/25V_4
PC54 SW@1200p/50V_4
DCR(max)=10mohm
PL10 SW@1.0uH/11A_7X7X3
PR157 SW@SHORT_PAD_6
PC147 SW@0.1u/50V_6
PR158 SW@10K/F_4
PG_1.5V_EN <43>
PR173 SW@51.1/F_4
PR170 SW@20K/F_4
PR162 SW@78.7K/F_4
PC145 SW@0.1u/25V
PC146 SW@10u/10V_8
PC48 SW@10u/10V_8
V0=0.8*(R1+R2)/R2
VIN_SRC
PR49 SW@1M/F_6
PR46 SW@1M/F_6
change p/n
PQ6 SW@SWAO6402A
+1.5V_GPU
PR47 SW@SHORT_PAD_4
PQ7 SW@PDTC143TT
PR48 SW@1M/F_6
PQ8 SW@DMN601K-7
PC46 *SW@2.2n/50V_4
+1.8V_GPU
1.41A
PC47 SW@1u/10V_4
7/9 change power enable net name to +1.5V_GPU (ZY9B solution)
Add it for S3 leakage circuit
<36> MAINON_DIS_G
7/23 modify
PR192 1M/F_6
PR186 1M/F_6
<37,41,42,43> MAINON
PR195 *100K_4
PQ47 DTC144EUA
+3V
PR187 22_8
PQ41 DMN601K-7
+5V
PR172 22_8
PQ42 DMN601K-7
+1.1V_VTT
PR182 22_8
PQ43 DMN601K-7
+1.5V
PR197 22_8
PQ46 DMN601K-7
+1.05V
PR196 22_8
PQ45 DMN601K-7
+15V
PR189 1M/F_6
PQ40 DMN601K-7
MAINON_G
MAIND
MAIND <36,39,43>
PC163 *2.2n/50V_4
7/7 modify
Quanta Computer Inc.
PROJECT : ZR7
Size
Document Number
Discharge/1.8V)
Rev 1A
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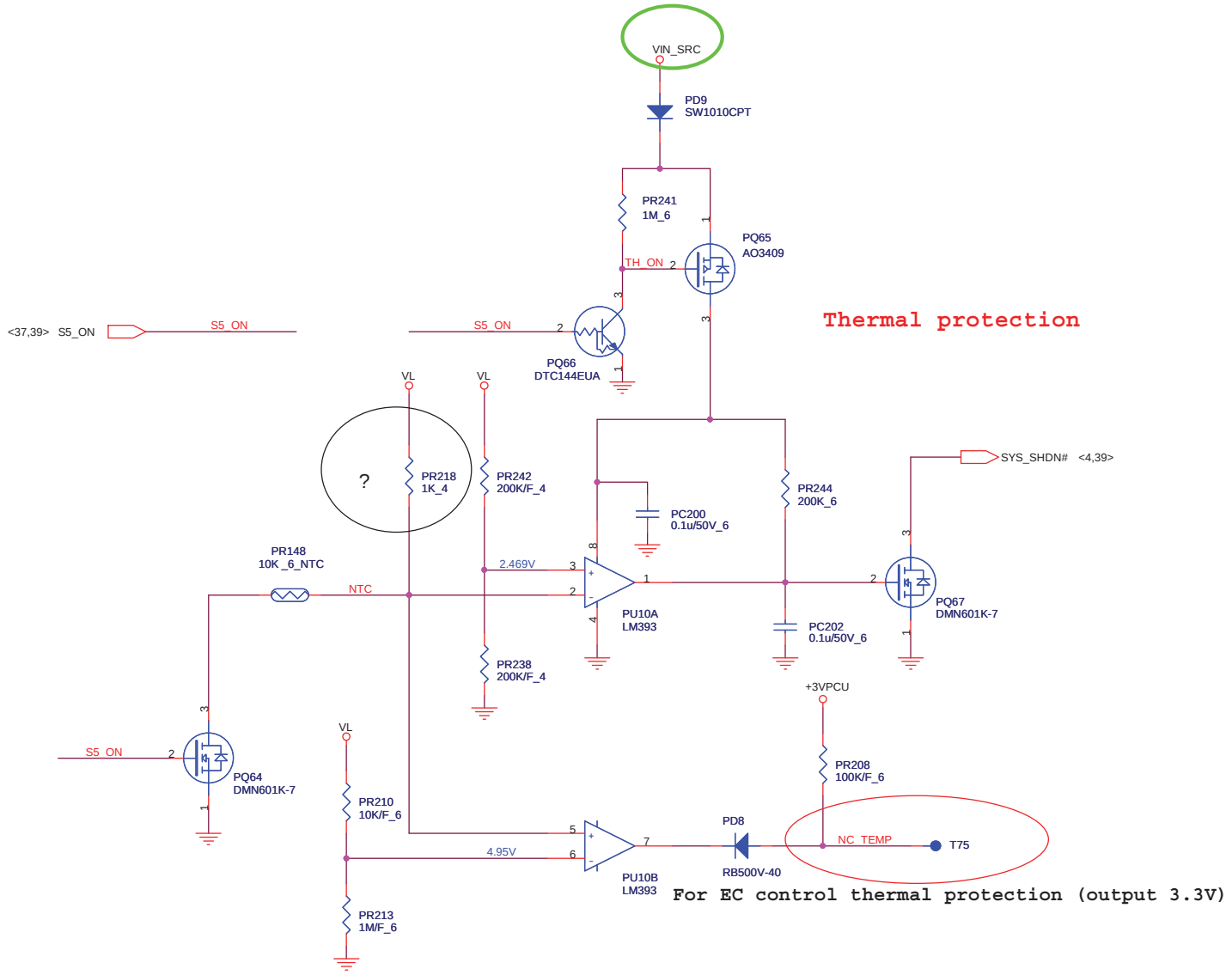

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.

PROJECT : ZR7

Size	Document Number	Rev
	Thermal Protection	1A

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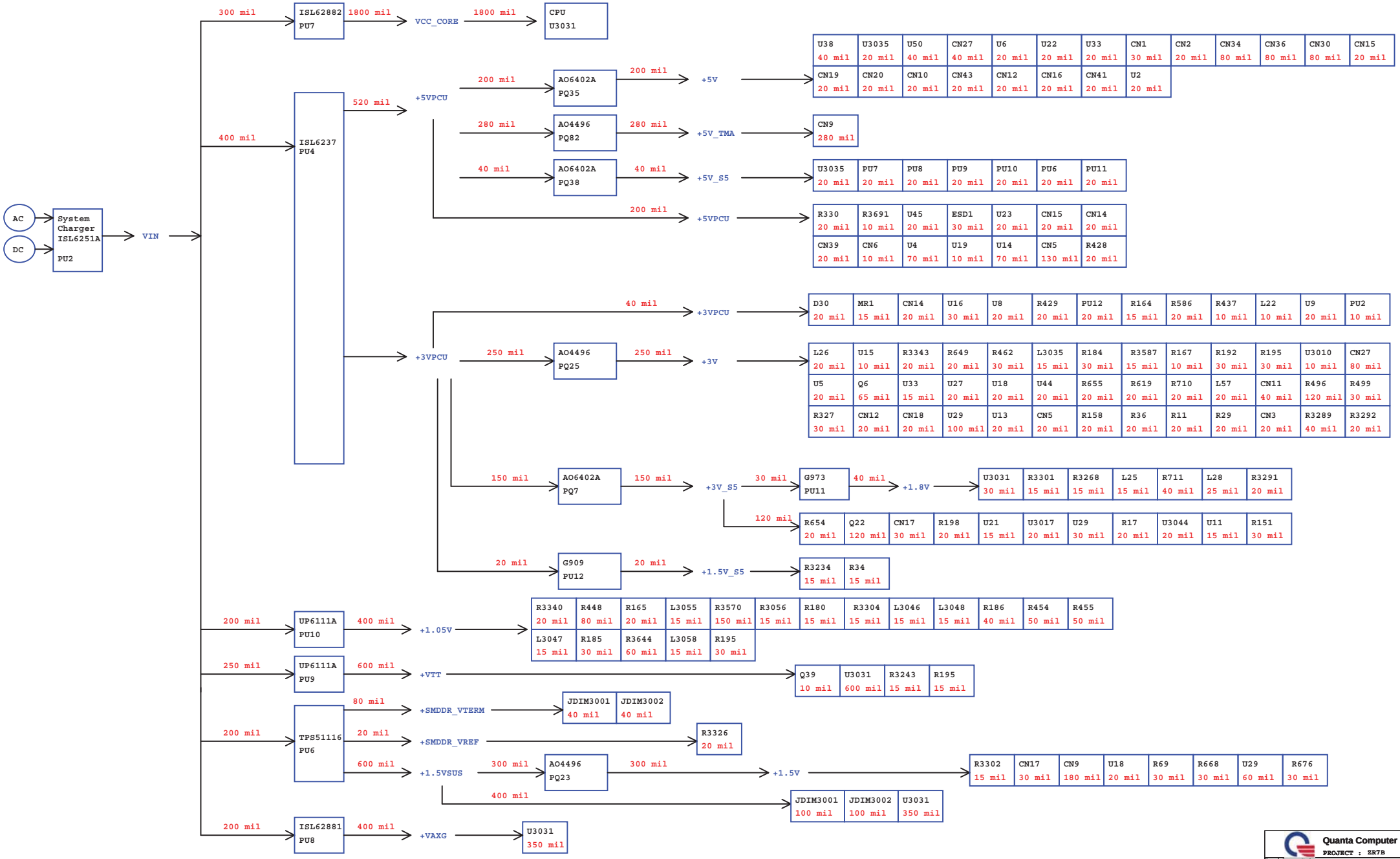

Quanta Computer Inc.

PROJECT : ZR7B

Size	Document Number	Rev
	POWER MANAGEMENT	1A

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Model	REV	CHANGE LIST	MODEL ZR7 FROM	To
ZR7B MB	1A	10/6 1. Change Hole13,14,15,16,18,19,20,21,27 for layout requirement__P35	X	1A
		2. Rename_All	X	1A
		3. Unstuff R203, R171__P27	X	1A
		10/12 1. PQ6 and +1V power system add SW# for power design change__P47	1A	B2A
		2. Swap VCORE1.2ID1 to pin AL13__P17	1A	B2A
		3. Change PR5, PR123, PR127, PR129 for power design change__P44	1A	B2A
		4. Unstuff PC68 for power design change__P43	1A	B2A
		5. Change Net name RST_GATE#_R to RST_GATE#__P36	1A	B2A
		6. Change U37 to 2M size__P9	1A	B2A
		7. Change PU7,PU12 for power design change__P47	1A	B2A
	2A	10/19 1. Change U36 P/N for PCH version update__P8-P13	1A	B2A
		2. Del R358 for ODD power control__P29	1A	B2A
		3. Unstuff R588,R268, Stuff R587,R273 for Speaker issue__P12, P30	1A	B2A
		4. Power design change	1A	B2A
		• PC223 change to use CC71004MX01	1A	B2A
		• PC201 change to use CC73301MX04	1A	B2A
		• PC194 change to use CC73301MX04	1A	B2A
		• PL11,PL12 change to use CV-18V0MZ04	1A	B2A
		• PC136, PC104, PC172, PC173, PC174,PC72 change to use CH6102K9A19	1A	B2A
		• PC68 change to use CH33306K915	1A	B2A
		• PR127 change to use CS34422FB00	1A	B2A
		• PR123 change to use CS44702FB13	1A	B2A
		• PR129 change to use CS34992FB01	1A	B2A
		• PR5 change to use CS42202FB10	1A	B2A
		• PC121 change to use CH61004M291	1A	B2A
		• PC21 change to use CH61004M291	1A	B2A
		• PL7 change to use CV-18V0MZ04	1A	B2A
		• PC25,PC134,PC30 change to use CH733RYE802	1A	B2A
		• PC118,PC119,PC127 change to use CH6102K9A19	1A	B2A
		• PC10,PC114 change to use CH61004M291	1A	B2A
		• PC211,PC212, PC96,PC148,PC146,PC48 change to use CH6102K9A19	1A	B2A
		10/28 1. R380,R376 PH with +3VPCU__P37	1A	B2A
		2. Mark +1V power system with sw#__P47	1A	B2A
		3. Mark +1.8V_GPU power system with sw#__P47	1A	B2A
		4. Change Net RF_LED_R and RF_LED# for BT and WLAN LED control__P37	1A	B2A
		5. Change CN4 P/N and footprint to 8pin for cost down__P24	1A	B2A
		6. Add R607, R608 for SW/B signal__P33	1A	B2A
		7. SMT product issues_All	1A	B2A
		• CN12,CN21 change footprint__P28	1A	B2A
		• PL10,PL17 change footprint__P47	1A	B2A
		• PU8 change footprint__P40	1A	B2A
		• PU4 change footprint__P46	1A	B2A
		• PU5 change footprint__P45	1A	B2A
		• Q36,Q40,Q42 change P/N__P31	1A	B2A
		• U34 change footprint__P27	1A	B2A
		9. Add R609 for vender suggest__P3	1A	B2A
		10. Add R610,R611,Q45,Q46, del R444, R443 for HDMI test__P25	1A	B2A
		11. Add R291,R315 for Acer requirement__P31	1A	B2A
		12. PC25, PC30, PC134 change value to 330u/2V_P44	1A	B2A
		11/12 1. Change bead from CX08T121000 to CX5AG121001 for vender cost down requirement__All	1A	B2A
		2. Change Bead from CX05T121000 to CX5AG121001 for vender cost down requirement__All	1A	B2A
		3. CN8 change P/N and footprint for ME design change__P34	1A	B2A
		4. Add Q45, Q46, R610, R611, del R443, R444 for HDMI issue__P34	1A	B2A
		5. Change PJ1 for ME design change__P38	1A	B2A
		6. Change HOLE18, 23, 6, 9, 27, 22, 17 and add HOLE30, 31 for machenical change_P35	1A	B2A
		7. Add R444, R443 1.5K for HDMI test__P25	1A	B2A
		8. Stuff L32, L35, L36, L38, Unstuff R230, R229, R321, R324, R316, R314, R306, R297 for EMI requirement __P34	1A	B2A
		9. Change R494, R520 from 0ohm to bead for EMI requirement __P34	1A	B2A
		10. Change R419 from 680ohm to 51ohm for ATI design change __P18	1A	B2A
		11/17 1. Remove 30#, Add MP# for separate different parts between Madison and Park__All	1A	B2A
		2. Remove Power Short Pad__All	1A	B2A
		3. Add PC232 for power design change__P38	1A	B2A
		4. Add Q47,R642 ,R542 for WIFI LED__P33	1A	B2A
		5. Change U16 P/N for update LAN chip version__P33	1A	B2A
		6. Change PJ1, CN8, CN4, RT1, CN14 for ODD, RTC, Battery connector change__All	1A	B2A
	3A	11/18 1. Swap L38 for layout requirement__P34	1A	B2A
		2. Change CN9 P/N and footprint for ME issue__P32	1A	B2A
		3. Change HOLE18, 23, 6, 9, 27, 22, 17 for layout requirement_P35	1A	B2A
		4. Power design change		
		• PR128, PR102, PR101, PR158, PR110, PR111, PR151, PL8, PL9, PR117, PL13, PR82 change P/N for power design change_All	B2A	C3A
		• Del PC68 for power design change_All	B2A	C3A
		• Add PC190 for power design change_All	B2A	C3A
		12/9 1. Change PR17, PR18, PC232 for Power design change__P38	B2A	C3A
		2. Del Q36, R455 and R441, Q33 change mark__P25	B2A	C3A
		3. R22,R23,R25,R27,R47,R65 change mark to MP#__P18	B2A	C3A
		4. Change R92, C565 location for ATI design change__P18	B2A	C3A
		5. Reserve R639 and add HDMI_HPD_PCH# for EC requirement__P9,P25	B2A	C3A
		12/18 1. Add R455,R612 PCH strap pin __P9	B2A	C3A
		2. Del 0ohm_0402: R10,R11,R15,R14,R83,R402,R388,R90,R91,R107,R144, R190,R199,R198,R220,R231,R248,R256,R273,R363, R369,R393,R394,R387,R437,R438,R400,R401,R501, R503,R526,R532,R548,R550,R552,R553,R554,R555, R556,R590,R606__All	B2A	C3A
		3. Del 0ohm_0603: R493,R122,R139,R148,R173,R174,R175,R176,R218, R219,R226,R228,R255,R232,R234,R235,R236,R237, R244,R264,R267,R284,R307,R545,R558,R581,R587__All	B2A	C3A
		4. U14 change footprint for PM requirement__P26	B2A	C3A
		5. Del R268,R588 for Audio I/O power level__P31	B2A	C3A
		6. Add R590 for LAN design change__P26	B2A	C3A
		7. Add R643 for W/L LED design change__P33	B2A	C3A
		8. SMTPE requirement	B2A	C3A
		*JHIM1 change footprint	B2A	C3A
		*PU3 change footprint	B2A	C3A
		*PR130 change footprint	B2A	C3A
		12/22 1. Cahnge Hole18, Hole23 for layout modify__P35	B2A	C3A
		12/24 1. R455 & R612 reconnect_P9	B2A	C3A
		2. R552/R553/R554/R555/R556 change back to 0 ohm for black screen issue verify_P28	B2A	C3A
		3. CN9 footprint change footprint_P32	B2A	C3A
		4. Update VRAM table and add VRAM# mark_P23	B2A	C3A
		5. EMI solution	B2A	C3A
		• R90 & R91 change to unstuff , L13 stuff._P24	B2A	C3A
		• Add R614 on LVDS_BRIGHT_P24	B2A	C3A
		• Adding C813 for VIN	B2A	C3A
		• Adding C814,C815,C816,C817,C818,C819,C820,C821 for VIN_SRC	B2A	C3A
		• Adding C822 for CSOP_1,PC102 change to stuff	B2A	C3A
		• Adding C823,C824,C825,C826,C827 for VIN_SRC	B2A	C3A
		• Add C828 to +3V	B2A	C3A
		• Change R614 to bead_P24	B2A	C3A
		6. Add F1 & F2 for safety.	B2A	C3A
		7. Add JP4 and delete JP5 for for change VGPU_IO source	B2A	C3A
		8. Change PR55 to 2.7K for Power change design_P40	B2A	C3A
		9. Add 30# for 3G function_All	B2A	C3A
	4A	12/31 1. U28 change to 512K, U37 change to 4M for BIOS design change_P9,P37		
		2. Change R328,R329,R330,R331,R334,R335 value for LED Brightness fine turn_P33		
		3. Stuff PR274,unstuff PR136, PR275 for change VGPU_IO source_P45		
		1/5 1. Reserve Board_ID PAD and unstuff R629,R630,R631,R632,R633,R634 _P10		
		2. Remove R417,R413,Q30,Q31 for costdown_P23,P37		
		3. Add trace VGA_THERM#_P23,P37		
		4. NONE		
		5. D10, F1 replace location_P24		
		6. Stuff R99, Change Q6<P/N modify> location for dGPU_SELECT_R control design change_P24		

2010/01/11
1. unstuff R486
2. R244 change from shortpad to RC0603 and unstuff.
3. C482 change from cap to 0 ohm resistor.

2010/01/18
1. delete PAD of U11/U12/U14
2. PR1
3. PD# PU change from +3V to +5VA & R599 change to 1K ohm resistor.

2010/01/19
1. PQ7 changes to RA001430249
2. PR1
3. remove shortpad R139/R148/R144
4. R152/R154/R259 change to SHORTPAD
5. R78 connect from +3V to +3V_D and R75 change to Unstuff.
6. F1/F2 update P/N.

2010/01/20
1. Unstuff R552/R553/R554/R555/R556
2. L23/L24/L25/R221/R249/R260/R305/R241/R242/R29/R32/R482/R544/ change to SHORTPAD
3. BOM for Board-ID,check again.

2010/01/21
1. add C829/EC1/EC2
2. Delete U30/C189
3. Delete D21/D22 , ADD Q36/Q39
4. Change PR21 to CS-2203J913
5. Change PC18 to CH22206K917
6. Unstuff<C815/C816/C817/C818/C820/C821/C823/C824/C825/C826/C827>

2010/01/22
1. R49/R101 change to SHORTPAD
2. Delete C829
3. C816/C818/C819/C820 change net and stuff.
4. Q36/Q39 should be always @ NOT SMB

2010/02/03
1. C777/PC190/PC1 update P/N & description.
2. PR222 Value change back to 0_4

2010/02/04
1. PR222 change to SHORTPAD
2. delete Q36/Q39 , add D21/D22, and reserve PAD of R615

2010/03/05
1. Delete PD2
2. PR101 & PR102 change P/N.

PR1 SHORT0603
PR44 SHORT0603
PR36 SHORT0402
PR72 SHORT0603
PR62 SHORT0402
PR81 SHORT0603
PR68 SHORT0402
PR115 SHORT0603
PR99 SHORT0402
PR154 SHORT0603
PR105 SHORT0402
PR156 SHORT0603
PR107 SHORT0402
PR206 SHORT0603
PR108 SHORT0402
PR240 SHORT0603
PR113 SHORT0402
PR245 SHORT0603
PR161 SHORT0402
PR250 SHORT0603
PR167 SHORT0402
PR254 SHORT0603
PR176 SHORT0402
PR257 SHORT0603
PR179 SHORT0402
PR266 SHORT0603
PR185 SHORT0402
PR270 SHORT0603
PR198 SHORT0402
PR60 SHORT0805
PR214 SHORT0402
PR120 SHORT0402
PR222 SHORT0402
PR199 SHORT0603
PR227 SHORT0402
PR200 SHORT0603
PR228 SHORT0402
PR230 SHORT0402
PR239 SHORT0402
PR248
PR249
PR251 SHORT0402
PR252 SHORT0402

SHORT0603
PR44 SHORT0603
PR36 SHORT0402
PR72 SHORT0603
PR62 SHORT0402
PR81 SHORT0603
PR68 SHORT0402
PR115 SHORT0603
PR99 SHORT0402
PR154 SHORT0603
PR105 SHORT0402
PR156 SHORT0603
PR107 SHORT0402
PR206 SHORT0603
PR108 SHORT0402
PR240 SHORT0603
PR113 SHORT0402
PR245 SHORT0603
PR161 SHORT0402
PR250 SHORT0603
PR167 SHORT0402
PR254 SHORT0603
PR176 SHORT0402
PR257 SHORT0603
PR179 SHORT0402
PR266 SHORT0603
PR185 SHORT0402
PR270 SHORT0603
PR198 SHORT0402
PR60 SHORT0805
PR214 SHORT0402
PR120 SHORT0402
PR222 SHORT0402
PR199 SHORT0603
PR227 SHORT0402
PR200 SHORT0603
PR228 SHORT0402

PR157 SHORT0603

PR230 SHORT0402

PR159 SHORT0402

PR239 SHORT0402

PR47 SHORT0402

PR248 SHORT0402
PR249 SHORT0402
PR251 SHORT0402
PR252 SHORT0402

Quanta Computer Inc. PROJECT : ZR7 Change list2	DOC NO.	PROJECT MODEL :	ZR7B	APPROVED BY:		DATE:	2009/12/24
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